Intronics Power ®

Low Cost/High Accuracy 18-Bit D/A Converter

DAC1146

FEATURES
- Integral Nonlinearity: ±0.00076% FSR max
- Differential Nonlinearity: ±0.00076% FSR max
- Low Differential Nonlinearity T.C.: ±1ppm/°C max
- Wide Power Supply Operation: ±11.5V to ±16V
- Fast Settling: 6µs to ±0.00076% FSR
- Small Size 2" × 2" × 0.4"

APPLICATIONS
- Automatic Test Equipment
- Digital Audio
- Sonar
- Robotics
- Nuclear Instrumentation

GENERAL DESCRIPTION

The DAC1146 is a low cost, 18-bit resolution (1 part in 262,144), digital-to-analog converter that provides high accuracy, high stability and is contained in a 2" × 2" × 0.4" module.

Integral and differential nonlinearity are both guaranteed at ±0.00076% FSR maximum. Additional guaranteed performance features include: differential nonlinearity T.C. ±1ppm/°C maximum, offset T.C. ±30µV/°C maximum, gain T.C. ±12ppm/°C maximum, bipolar offset T.C. ±7ppm/°C maximum.

The DAC1146 makes use of CMOS integrated circuits, thin-film resistor technology and proprietary CMOS current-steering switches to obtain high resolution, high reliability and small size. The calculated MTBF for the DAC1146 is 275,445 hours, per Mil Handbook 217C.

The DAC1146 can operate with power supplies ranging from ±11.5V to ±16.0V. An internal precision reference is provided, an external reference can be used. The external reference voltage input range is −12V to +12V. The analog output ranges include: +5V, +10V, ±5V, ±10V, −2mA and ±1mA, and are selectable via pin programming (see Figure 1). Digital input coding for unipolar operation is true binary, bipolar input coding is offset binary or 2's complement.

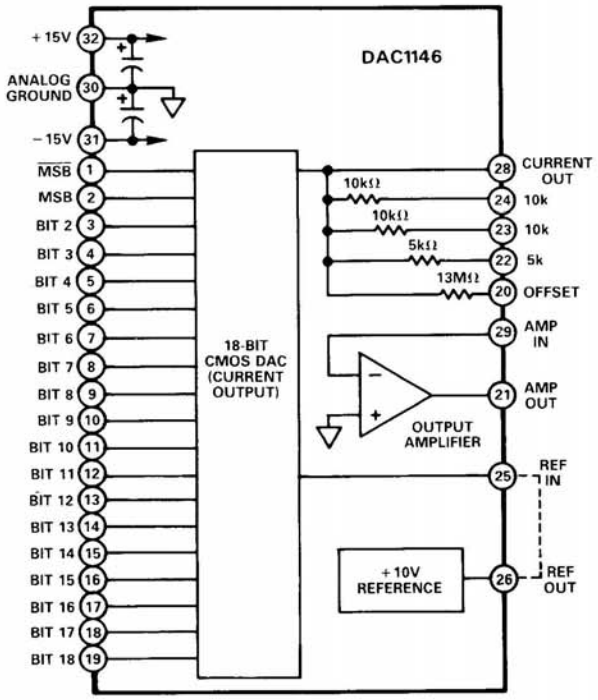

Figure 1. DAC1146 Functional Block Diagram

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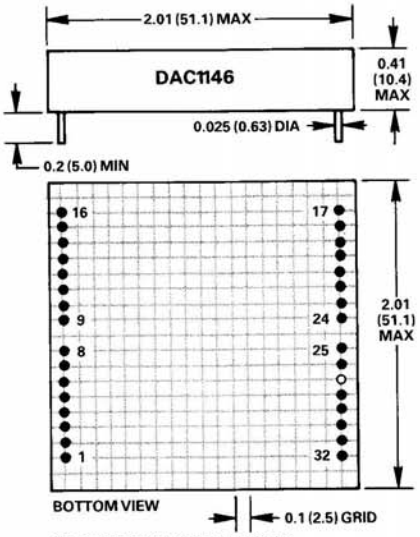
SPECIFICATIONS (typical @ +25°C, V_S = ±15V, V_{REF} = +10V unless otherwise specified)

MODEL	DAC1146
RESOLUTION	18 Bits
ACCURACY	
Integral Nonlinearity	± 0.00076% FSR[1](max)
Differential Nonlinearity	± 0.00076% FSR[1](max)
Monotonic (16 Bits)	Guaranteed
Offset[2]	Adjustable to Zero
Gain[2]	Adjustable to Full Scale
STABILITY	
Differential Nonlinearity	± 1ppm/°C (max)
Offset	± 30µV/°C (max)
Bipolar Offset	± 7ppm/°C (max)
Gain	± 12ppm/°C (max)
STABILITY, Long Term (ppm/1000 hr)	
Differential Nonlinearity	± 1ppm
Offset	± 3ppm
Bipolar Offset	± 3ppm
Gain	± 12ppm
REFERENCE VOLTAGE (V_{REF})	
Output Voltage	+ 10.00V ± 0.3% (max)
Output Current	2mA (max)
Ext. Ref Voltage Range[3]	− 12V to + 12V
Input Resistance	12kΩ
DYNAMIC PERFORMANCE[4]	
Settling Time to ± 0.00076% Voltage, Full Scale Step	
Unipolar (10V)	6µs
Bipolar (± 10V)	12µs
Voltage, LSB Step	3µs
Current	2µs
DIGITAL INPUTS	CMOS, TTL Compatible
Codes	
Unipolar	Binary (BIN)
Bipolar	Offset Binary (OBIN), Two's Complement
ANALOG OUTPUT	
Voltage	+ 5V, + 10V, ± 5V, ± 10V
Current	− 2mA, ± 1mA
Voltage Compliance	± 500mV
Noise (100kHz B.W.)	30µV rms
POWER REQUIREMENTS	
Voltage (Rated Performance)	± 15V (± 5%)
Voltage (Operating)	± 11.5V to ± 16.0V
Supply Current Drain ± 15V	+ 15mA, − 25mA
Total Power @ V_S = ± 15V	600mW
POWER SUPPLY SENSITIVITY	
Offset	0.001%/% ± V_S
Gain	0.001%/% ± V_S
TEMPERATURE RANGE	
Rated Performance	0 to + 70°C
Operating	− 25°C to + 85°C
Relative Humidity	Meets MIL STD 202E, Method 103B
SIZE	2" × 2" × 0.4" (50.8 × 50.8 × 10.16mm)
Weight	33g

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS

MATING CONNECTORS AC1584-3 (2 REQUIRED)

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{\text{MSB}}$	32	+15V
2	MSB	31	−15V
3	BIT 2	30	ANALOG GROUND
4	BIT 3	29	AMP IN
5	BIT 4	28	CURRENT OUT
6	BIT 5	27	N.C.
7	BIT 6	26	REFERENCE OUT
8	BIT 7	25	REFERENCE IN
9	BIT 8	24	10k
10	BIT 9	23	10k
11	BIT 10	22	5k
12	BIT 11	21	AMP OUT
13	BIT 12	20	OFFSET
14	BIT 13	19	BIT 18 (LSB)
15	BIT 14	18	BIT 17
16	BIT 15	17	BIT 16

NOTES
[1]FSR means Full Scale Range.
[2]Offset and gain are adjustable to zero by means of external potentiometers. See Figure 2 for proper connections.
[3]Rated performance is specified with + 10.0V reference.
[4]See Figure 5 for settling time curves.
Recommended Power Supply: Analog Devices Model 904.
Specifications subject to change without notice.

ANALOG OUTPUT RANGE

In the unipolar mode the DAC1146 provides an output current of −2mA. In the bipolar mode the DAC output current is offset by 1mA, (by connecting pin 25 to pin 24) for an output of ±1mA.

The DAC can be pin programmed for +5V, +10V, ±5V and ±10V by converting the DAC's current output to a voltage. To program the DAC for voltage output ranges (see Figure 1, Figure 2 and Table I).

Output Voltage Range	Input Code[1]	Connect Pin[2] 25 to Pin	Connect Pin 28 to Pin	Connect Pin 21 to Pin(s)
+5V	BIN		29	22, 23, 24
+10V	BIN		29	23, 24
±5V	OBIN, 2's Comp	24	29	22
±10V	OBIN, 2's Comp	24	29	23

[1]For BIN or OBIN codes connect $\overline{MSB}$ to ground.
For 2's comp code connect MSB to +5V system power.
[2]Connect Pin 25 through a 50Ω potentiometer to either internal reference (Pin 26) or an external reference.

Table I. Analog Output Range Pin Programming

OFFSET AND GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 2. Proper offset and gain calibration requires great care and the use of extremely sensitive and accurate measurement instruments. These instruments should be capable of measuring to within 1μV of the adjusted output voltage at both ends of the range. The potentiometers selected should be good quality Cermet type. Multi-turn potentiometers having ten to fifteen turns and 100ppm/°C temperature coefficients will be adequate. The temperature coefficients contributed by these Cermet potentiometers will be less than 0.1ppm/°C.

For unipolar mode, apply a digital input code of all "0's" and adjust the offset potentiometer until a 0.00000V output is obtained (see Table II). Once the appropriate offset adjustment has been made, apply a digital input code of all "1's", and adjust the gain potentiometer until the plus full scale output is obtained (see Table II).

For bipolar mode, apply a digital input code of 100 . . . 00 and adjust the offset potentiometer until a 0.00000V output is obtained (see Table II). Once the appropriate offset adjustment has been made, apply a digital input of all "1's", and adjust the gain potentiometer until the proper plus full scale output is obtained.

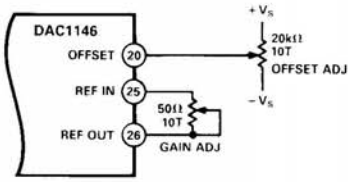


Figure 2. Offset & Gain Calibration

	Code 000 . . . 00	Code 111 . . . 11
Unipolar		
+5V	0.00000V	+4.999981V
+10V	0.00000V	+9.999962V
	Code 100 . . . 00	**Code 111 . . . 11**
Bipolar		
±5V	0.00000V	+4.999962V
±10V	0.00000V	+9.999924V

Table II. Full Scale Calibrated Output Voltages

PRECISION LOW DRIFT VOLTAGE OUTPUT

The internal output amplifier of the DAC1146 is optimized for high speed applications like digital audio and sonar, that require fast settling time. An external precision operational amplifier like the AD OP-07 can be applied when low offset drift is important. Simply connect the current output (Pin 28) to the inverting input of the amplifier. This connection should be made as close as possible to the DAC. Connect the proper feedback resistors as shown in last two columns of Table I. To avoid decreasing the gain drift performance of the DAC always use the internal feedback resistors, since they are matched to the internal current weighting resistors of the DAC (see Figure 3).

The current drift of the DAC1146 is typically 350pA/°C from +15°C to +35°C. When using the AD OP-07, the total drift of the output signal will be less than 2μV/°C.

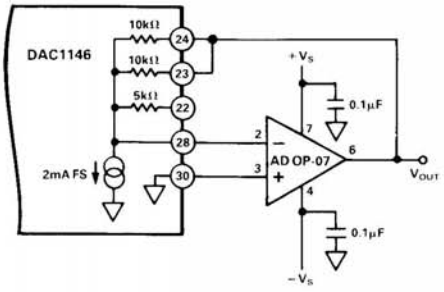


Figure 3. Low Drift Voltage Output (+10V) Application

DIFFERENTIAL LINEARITY ADJUSTMENT

Each DAC1146 has been factory calibrated and tested to achieve the performance indicated in the electrical specifications. Before attempting recalibration, it is imperative that the circuit be checked to confirm that all precautions have been taken to insure proper application. The DAC is trimmed by comparing a bit to the sum of all lower bits, and adjusted if necessary, for a one LSB positive difference. The top four bits can be trimmed using the procedure outlined on next page. A differential voltmeter capable of 100μV full scale should be connected to amp out of the DAC. A Fluke 895A or equivalent is recommended (see Figure 4).

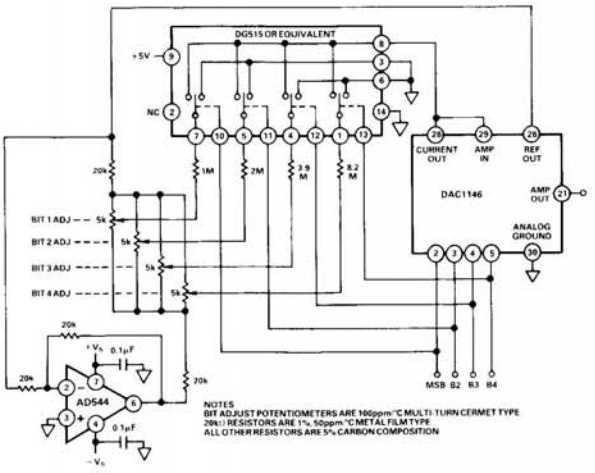


Figure 4. Optional Differential Linearity Adjustment Circuit

1. Start with Bit 4, proceed to Bits 3, 2 and 1 by repeating steps 2 through 5. Set Bits 17 and 18 to "0" for this entire rocedure.
2. Set all digital inputs less significant than the bit being adjusted to "1"; set all others to "0".
3. Read the output voltage by nulling the voltmeter.
4. Set the digital input for the bit being adjusted to "1", set all others to "0".
5. Read the output voltage by nulling the voltmeter. This reading should be equal to that of Step 3 plus 153μV (10V FSR). If not, adjust the bit.
6. Retrim gain.

DIGITAL AUDIO APPLICATION

When using a DAC to reconstruct an audio signal, emphasis is placed on important audio parameters. These parameters include: Total Harmonic Distortion, Dynamic Range and Settling Time.

Settling Time: Settling time is the total time for the output to settle within an error band around its final value after a change in the input. Settling times for the DAC1146 are specified to ±0.00076% of full-scale for any step change (see Figure 5).

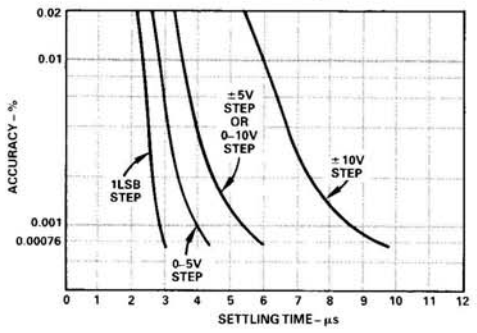


Figure 5. Voltage Settling Time vs Accuracy

Dynamic Range: The DAC1146 has a typical dynamic range of 96dB for a 16-bit input and 100dB for an 18-bit input. The theoretical dynamic range can be expressed as 6dB X N, where N is the number of bits. The theoretical limit would indicate a dynamic range of 108dB for an 18-bit input, however linearity, noise and other errors limit the useful dynamic range to 100dB at 18 bits.

Total Harmonic Distortion: When the DAC1146 is used at 16 bits of resolution with a deglitcher as shown in Figure 6, the Total Harmonic Distortion (THD) for a full scale signal over the entire audio range 20Hz to 20kHz is typically less than 0.002% or −94dB.

Total Harmonic Distortion is defined as the ratio of the square root of the sum of the squares of the rms harmonic value to the rms fundamental values and is expressed in percent dB.

The THD can be calculated from the following formula and verified by testing (see Figure 6).

$$THD = \frac{\text{RMS Error}}{\text{RMS Signal}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}\left[E_L(i) + E_Q(i)\right]^2}}{\text{RMS Signal}} \times 100\%$$

where N is the number of samples.
$E_L(i)$ is the linearity error of the DAC at each sample point.
$E_Q(i)$ is the quantization error of the DAC at each sample point.

THD TESTING

When testing for THD the test equipment used must be distortion free so as not to mask the true performance of the device under test. The test circuit (see Figure 6) will produce a negligible amount of distortion when generating a test signal.

The PROM contains one cycle of a computer generated sine wave. Frequency select switches program the adder with the number of codes that it should skip on each count. This selection allows any of 2048 discrete frequencies between 12Hz and 25kHz to be generated with a constant 50kHz update rate. The DAC output is deglitched, and displayed on the spectrum analyzer. Total Harmonic Distortion can be computed by comparing the amplitude of the fundamental frequency with the amplitudes of the harmonics.

TYPICAL THD TEST RESULTS

Dynamic Range	16-Bit Resolution	18-Bit Resolution
Dynamic Range	96dB	100dB
THD at FS	0.002% (−94dB)	0.0015% (−96dB)
THD at −15dB	0.01% (−80dB)	0.0075% (−82dB)
THD at −20dB	0.02% (−74dB)	0.015% (−76dB)
THD at −30dB	0.06% (−64dB)	0.045% (−67dB)

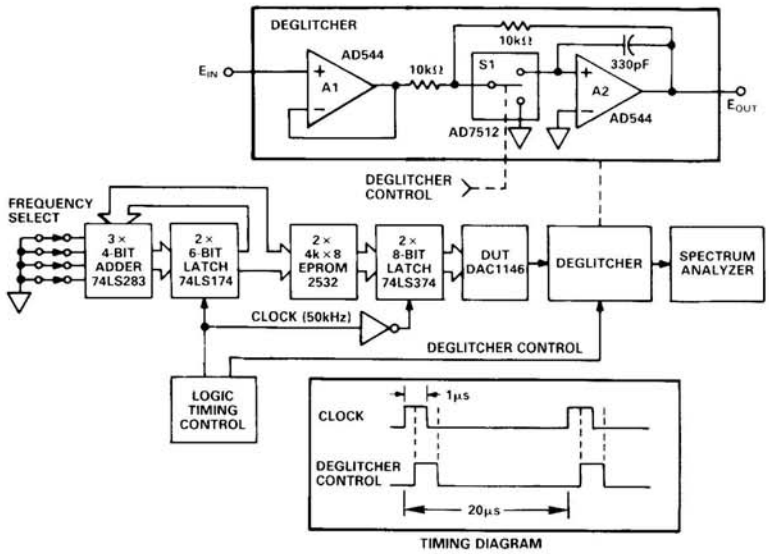


Figure 6. Block Diagram Harmonic Distortion Test Circuit