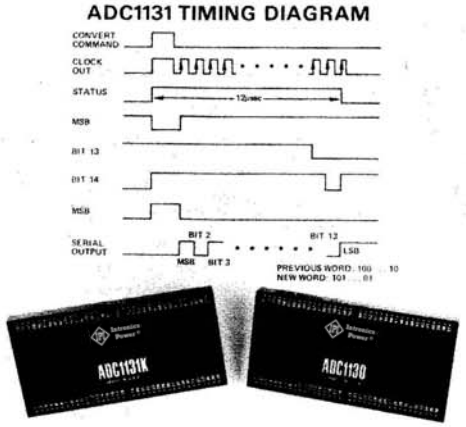
Intronics Power ®

14-Bit High Speed Analog to Digital Converters

ADC1130, ADC1131

FEATURES
- 14-BIT Resolution and Accuracy
- Fast 12μs Conversion Time (ADC1131J/K)
- Low 10ppm/°C Maximum Gain TC
- User Choice of Input Range
- No Missing Codes

APPLICATIONS
- Wide Band Data Digitizing
- Multi-Channel Computer Interface
- High Accuracy Data Acquisition
- X-Ray Tomography
- Nuclear Accelerator Instrumentation



GENERAL DESCRIPTION

The ADC1130 and ADC1131 are high speed analog-to-digital converters packaged in a small 2″ x 4″ x 0.4″ (51 x 102 x 10mm) module, which perform complete 14-bit conversions in 25μs and 12μs respectively. Using the successive approximations technique, they convert analog input voltages into natural binary, offset binary, or two's complement coded outputs. Data outputs are provided in both parallel and non-return-to-zero serial form.

Four analog input ranges are available: 0 to +20V, 0 to +10V, ±10V, ±5V. The user selects the desired range by making appropriate connections to the module terminals. The ADC1130 and ADC1131 can also be connected so as to perform conversions of less than 14 bit resolution with a proportionate decrease in conversion time.

TIMING

As shown in Figure 1, the leading edge of the convert command set the MSB output to Logic "0" and the CLOCK OUT, STATUS, $\overline{\text{MSB}}$, and BIT 2 through BIT 12 outputs to Logic "1". Nothing further happens until the convert command returns to Logic "0", at which time the clock starts to run and the conversion proceeds.

With the MSB in the Logic "0" state, the internal digital-to-analog converter's output is compared with the analog input. If the D/A output is less than the analog input, the first "0" to "1" clock transition resets the MSB to Logic "1". If the D/A output is greater than the analog input, the MSB remains at Logic "0".

The first "0" to "1" clock transition also sets the BIT 2 output to Logic "0" and another comparison is made. This process continues through each successive bit until the BIT 14 (LSB) comparison is completed. At this point the STATUS and CLOCK OUT return to Logic "0" and the conversion cycle ends.

The serial data output is of the non-return-to-zero (NRZ) forma The data is available, MSB first, 20ns after each of the fourteen "0" to "1" clock transitions.

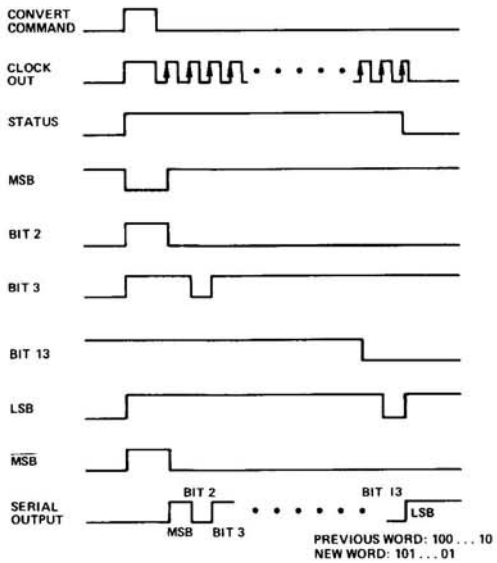


Figure 1. Timing Diagram

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SPECIFICATIONS (typical @ +25°C unless otherwise noted)

MODEL	HIGH SPEED 12μs ADC1131 J	K	MEDIUM SPEED 25μs ADC1130
RESOLUTION, BITS	14	14	14
CONVERSION TIME (max)	12μs	12μs	25μs
ACCURACY			
Integral Nonlinearity Error (LSB)	±1/2 (max)	*	*
Differential Nonlinearity Error (LSB)	±1/2 (1 max)	±1/2 (max)	±1/2 (1 max)
Missing Codes	No missing codes	*	*
TEMPERATURE COEFFICIENTS			
Gain ppm/°C	±12 (max)	±7 (+10 max)	±12 max
Unipolar Offset	±0.7 (±3 max)	*	*
Bipolar Offset	±3 (±7 max)	*	*
INPUT VOLTAGE RANGES	±5V, ±10V, +10V, +20V	*	*
INPUT IMPEDANCE (10V RANGE)	2500Ω	*	*
CONVERT COMMAND	Positive Pulse, 200ns min, 400ns max Leading Edge Resets, Trailing Edge Starts, TTL/DTL Compatible	*	*
PARALLEL DATA OUTPUT			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary, Two's Complement	*	*
SERIAL DATA OUTPUT			
Unipolar	Positive True Binary	*	*
Bipolar	Positive True Offset Binary	*	*
STATUS OUTPUT	"1" During Conversion. Complement also available TTL/DTL Compatible.	*	*
LOGIC FANOUTS AND LOADINGS			
Convert Command Input	1TTL Unit Load	*	*
Clock Input	3TTL Unit Loads	*	*
Short Cycle Input	1TTL Unit Load	*	*
Parallel Data Outputs	3TTL Unit Loads/Bit	*	*
Serial Data Output	8TTL Unit Loads	*	*
STATUS Output	2TTL Unit Loads	*	*
$\overline{\text{STATUS}}$ Output	12TTL Unit Loads	*	*
Clock Output	4TTL Unit Loads	*	*
POWER REQUIREMENTS	+15V ±5% @ 40mA	*	*
	-15V ±5% @ 60mA	*	*
	+5V ±5% @ 250mA	*	*
POWER SUPPLY SENSITIVITY			
To ±15V Tracking Supplies			
Gain	±4.5ppm/%Δ V_S	*	*
Zero	±4.5ppm/%Δ V_S	*	*
To ±15V Non-Tracking Supplies			
Gain	±10ppm/%Δ V_S	*	*
Zero	±7ppm/%Δ V_S	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	*
Storage	-55°C to +85°C	*	*

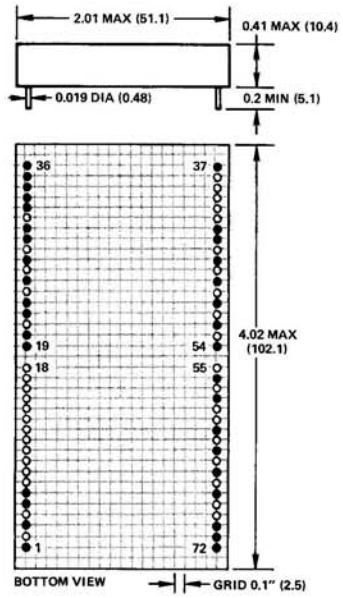
*Same Specifications as ADC1131J.

NOTES:
[1] Offset (zero) and gain errors are adjustable to zero by means of external potentiometers. See Figure 5 for proper connection.
[2] Recommended power supply: Analog Devices model 923.

Specifications subject to change without notice.

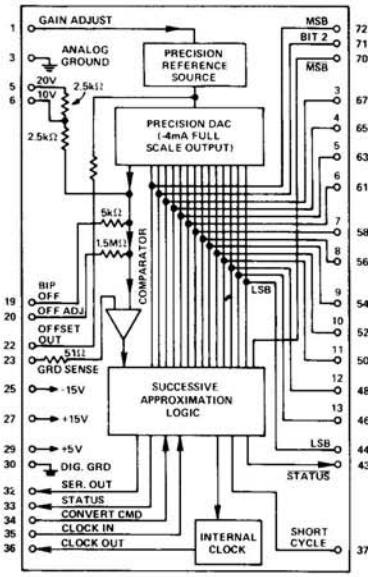
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE:
Terminal pins installed only in shaded hol locations.
Module weight: 3.5 ounces (99.3 grams).
All pins are gold plated half-hard brass (MIL–G–45204), 0.019" ±0.001" (0.48 ±0.03mm) dia.
For plug-in mounting card order Board No. AC1578.

BLOCK DIAGRAM AND PIN DESIGNATIONS



ANALOG INPUT CHARACTERISTICS

The input circuit of the ADC1130 and ADC1131 are shown in block diagram form.

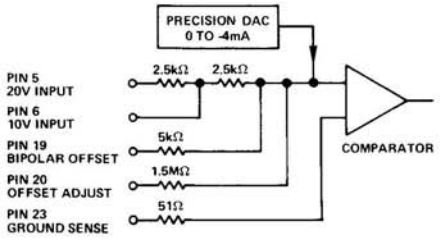


Figure 2. Input Circuit Block Diagram

When the converters are connected as a unipolar device, Pin 19 is left open circuit and, thus, no offset current is applied to the comparator input. The 0 to +10V input signal applied to Pin 6 (or the 0 to +20V input signal applied to Pin 5) develops a 0 to +4mA current which is compared to the 0 to -4mA output of the D/A converter. A voltage between +15V and -15V can be applied to Pin 20 from the wiper of a 100kΩ potentiometer to adjust the zero point by ±40LSB. To reduce the range of this trim padding resistors should be used.

With the offset output, Pin 22, connected to Pin 19, a +2mA offset current is applied to the comparator input. The ADC1130 and ADC1131 will then accept bipolar inputs of ±5V at Pin 6, or ±10V at Pin 5 and compare the 0 to +4mA sum of the offset and input signal currents to the 0 to -4mA D/A converter output. The offset adjustment potentiometer is once again used as described in the preceding paragraph.

Signal ground sense, Pin 23, should normally be jumpered to analog ground, Pin 3. In the event that an offset voltage is developed in the ground wiring, it may be possible to eliminate its effect by connecting Pin 23 directly to the signal or analog ground of the device feeding the analog input signal to the ADC. In any case, Pin 23 must not be left open.

If a high input impedance is required, it can be achieved by using a high speed operational amplifier as an input buffer.

PARALLEL DATA OUTPUT

These converters produce natural Binary Coded outputs when configured as a unipolar device. As a bipolar device, they can produce either Offset Binary or Two's Complement output codes. The most significant bit is represented by Pin 72 (MSB output) for Binary and Offset Binary codes, or by Pin 70 ($\overline{\text{MSB}}$ output) for the Two's Complement code. Tables I and II illustrate the relationship between analog input and digital output for all three codes.

ANALOG INPUT		DIGITAL OUTPUT
0 to +10V Range	0 to +20V Range	Binary Code
+9.9994V	+19.9988V	11111111111111
+5.0000V	+10.0000V	10000000000000
+1.2500V	+2.5000V	00100000000000
+0.0006V	+0.0012V	00000000000001
+0.0000V	+0.0000V	00000000000000

Table I. Nominal Unipolar Input-Output Relationships

±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.9994V	+9.9988V	11111111111111	01111111111111
+2.5000V	+5.0000V	11000000000000	01000000000000
+0.0006V	+0.0012V	10000000000001	00000000000001
+0.0000V	+0.0000V	10000000000000	00000000000000
-5.0000V	-10.0000V	00000000000000	10000000000000

Table II. Nominal Bipolar Input-Output Relationships

SERIAL DATA OUTPUT

The serial data output, available on Pin 32, is of the non-return-to-zero format. The data is transmitted MSB first and is Binary coded for unipolar units and Offset Binary coded for bipolar units.

Figure 3, shown below, indicates one method for transmitting data serially using only three wires (plus a digital ground). The data is clocked into a receiving shift register using the delayed clock output of the converter.

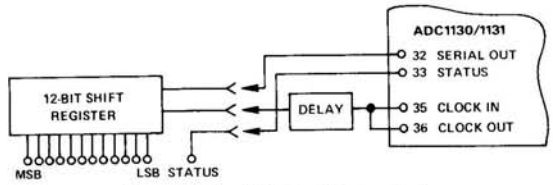


Figure 3. Serial Data Transmission

The timing diagram presented in Figure 4 shows that the converter's clock output must be delayed by an amount of time greater than or equal to the sum of the receiving shift register setup time plus the 20ns clock output to serial output delay.

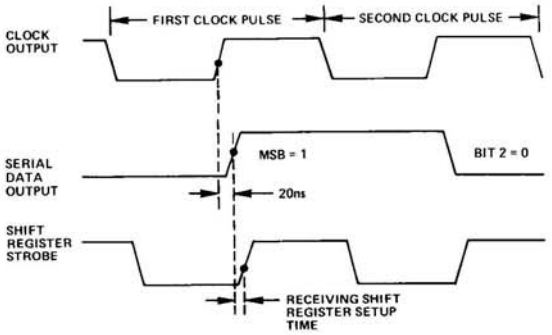


Figure 4. Serial Data Timing Diagram

The 50ns span between the time that the last serial output bit is available and the time that the STATUS output returns to zero insures that the data in the shift register will be valid on the "1" to "0" transition of the STATUS signal.

GAIN AND OFFSET ADJUSTMENTS

The potentiometers used for making gain and offset adjustments are connected as shown in Figure 5. Note that a jumper

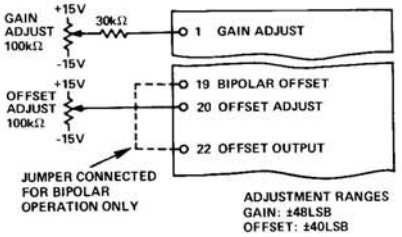


Figure 5. Adjustment Connections

is connected between Pin 19 and Pin 22 for bipolar operation; these pins *must* be left open for unipolar operation.

Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable. It should be capable of being set to within 1μV of the desired value at both ends of its range.

The gain and offset calibrations will be independent of each other if the offset adjustment is made first. These adjustments are not made with zero and full scale input signals and it may be helpful to understand why. An A/D converter will produce a given digital output for a small range of input signals, the nominal width of the range being one LSB. If the input test signal is set to a value which should cause the output of the converter to be on the verge of switching from one digital value to the adjacent digital value, the unit can be calibrated so that it does change values at just that point. With a high speed convert command rate and a visual display, these adjustments can be performed in a very accurate and sensitive way. Analog Devices' *Analog-Digital Conversion Notes* gives more detailed information on testing and calibrating A/D and D/A converters.

OFFSET CALIBRATION

For the 0 to +10V unipolar range set the input voltage precisely to +0.0003V; for 0 to +20V units set it to +0.0006V. Adjust the zero potentiometer until the converter is just on the verge of switching from 00 . . . . 0 to 00 . . . . 1.

For the ±5V bipolar range set the input voltage precisely to -4.9997V; for ±10V units set it to -9.9994V. Adjust the zero potentiometer until offset binary coded units are just on the verge of switching from 00 . . . . 0 to 00 . . . . 1 and two's complement coded units are just on the verge of switching from 100 . . . 0 to 100 . . . 1.

GAIN CALIBRATION

Set the input voltage precisely to +19.9982V for 0 to +20V units, +9.9991V for 0 to +10V units, +4.9991V for ±5V units, or +9.9982V for ±10V units. Note that these values are 1½LSB's less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11 . . . 0 to 11 . . . 1 and two's complement coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11.

POWER SUPPLY AND GROUNDING CONNECTIONS

These converters do not have an internal connection between analog power ground and digital ground and, thus, a connection must be provided in the external circuitry. The choice of an optimum "star" point for these grounds is an important consideration in the performance of the system. No strict rules can be given, only the general guidelines that the grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. One suggested approach is shown in Figure 6.

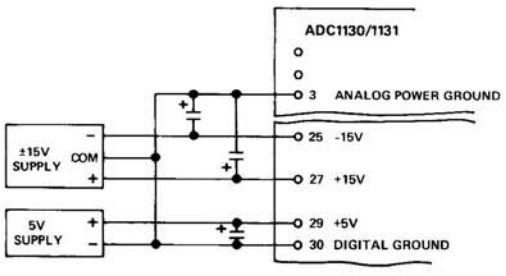


Figure 6. Power Supply and Grounding Connections

The ±15V and +5V power supplies must be externally bypassed with 15μF (+35V tantalum) capacitors. These capacitors should be connected between Pin 27 and Pin 3, between Pin 25 and Pin 3, and between Pin 29 and Pin 30. Capacitor connections should be made as close to the module pins as possible.

CLOCK CONNECTIONS

When the converters are used with their own internal clock, Pin 36 is simply jumpered to Pin 35. When the internal clock is not used, Pin 36 is grounded and an external clock capable of driving three TTL loads is connected to Pin 35. The convert command should be synchronized with the external clock.

REPETITIVE CONVERSIONS

When making repetitive conversions, a new convert command may be initiated any time after the "1" to "0" transition of the STATUS output. The $\overline{\text{STATUS}}$ output may not, however, be connected directly to the CONVERT COMMAND input for the purpose of automatically generating convert command pulses.

SHORT CYCLE CONNECTIONS

When the converters are operated as a 14-bit device, Pin 37 is left open. If, however, it is to perform conversions of less than 14 bits, Pin 37 is connected to the N+1 bit output (where N is the number of bits in the conversion). The conversion time in this mode of operation is T_C x N/14 where T_C is the conversion time of the particular model when operated at 14-bit resolution.

THE AC1578 MOUNTING CARD

The AC1578 mounting card is specifically designed to be used with Analog Devices high resolution, high speed analog-to-digital converters, models ADC1130 and ADC1131. This 4.5" X 3.56" (114 X 90mm) printed circuit card, shown in Figure 7, has sockets which allow the converter to be plugged directly onto it. It contains an input buffer that can be programmed using on-board jumpers to provide the input ranges of 0–10 volts, ±10 volts, or ±5 volts. Additionally, a 0–20 volt input range can be achieved by wiring the AC1578 without utilizing the buffer.

The analog information has been isolated from the digital information by the use of two separate connectors, one at the top (designated "P1") and one at the bottom (designated "P2") of the AC1578. Both connectors P1 and P2 are supplied with each card. Whenever feasible, the top connector should be used for analog interfacing to eliminate crosstalk.

Additional wiring information and calibration procedure are contained in a separate data sheet for the AC1578 which is shipped with the card and is available on request.

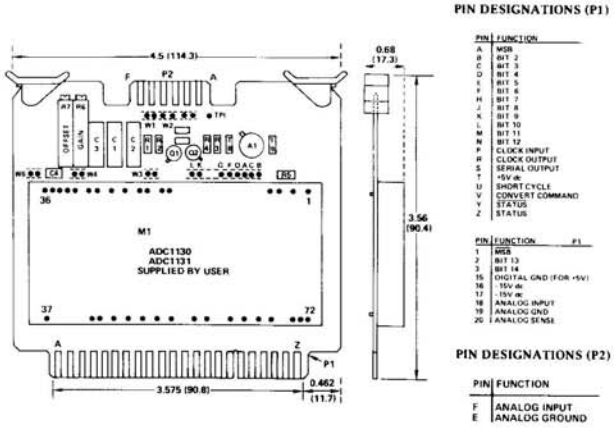


Figure 7. AC1578 Mounting Card

Intronics Power ®

Low Cost 16-Bit Analog-to-Digital Converter

ADC1140

FEATURES

- Guaranteed Nonlinearity: ±0.003% FSR max
- 35μs Maximum Conversion Time
- Small Size 2″ × 2″ × 0.4″
- Wide Power Supply Operation: ±12V to ±17V

APPLICATIONS

- Process Control Data Acquisition
- Seismic Data Acquisition
- Nuclear Instrumentation
- Medical Instrumentation
- Pulse Code Modulation Telemetry
- Industrial Scales
- Robotics

GENERAL DESCRIPTION

The ADC1140 is a low cost 16-bit successive-approximation analog-to-digital converter having a 35μs maximum conversion time. This converter provides high accuracy, high stability and low power consumption all in a 2″ × 2″ × 0.4″ module.

High accuracy performance such as integral and differential nonlinearity of ±0.003% FSR max are both guaranteed. Guaranteed stability such as differential nonlinearity TC of ±2ppm/°C maximum, offset TC of ±30μV/°C maximum, gain TC of ±12ppm/°C maximum and power supply sensitivity of ±0.002% of FSR/% V_S are also provided by the ADC1140.

The ADC1140 makes extensive use of both integrated circuit and thin-film components to obtain excellent performance, small size and low cost. The internal 16-bit DAC incorporates Analog Devices' proprietary thin-film resistor technology and proprietary CMOS current-steering switches. A low noise reference, low power comparator and low power successive-approximation register are also used to optimize the ADC1140's design (shown in Figure 1).

The ADC1140 can operate with power supplies ranging from ±12V to ±17V and has provisions for a user supplied external reference. Four analog input voltage ranges are selectable via pin programming: ±5V, ±10V, 0 to +5V and 0 to +10V. Bipolar coding is provided in the offset binary and two's complement formats with unipolar coding displayed in true binary.

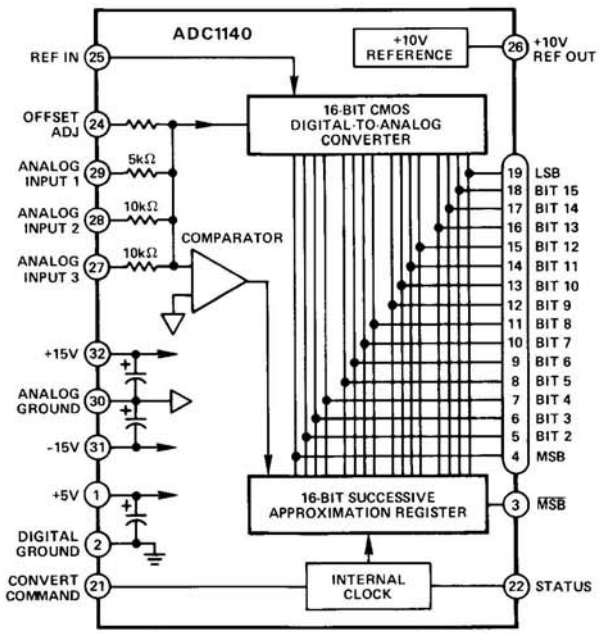


Figure 1. ADC1140 Functional Block Diagram

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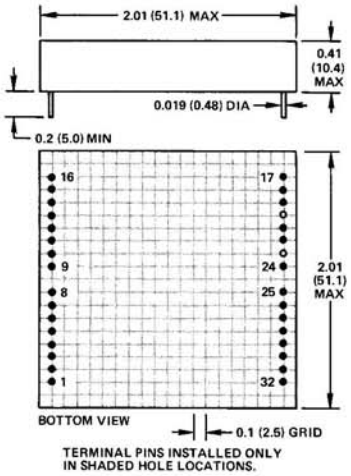
SPECIFICATIONS (typical @ +25°C $\pm V_S$ = ±15V, V_{CC} = +5V, V_{REF} = +10.0V unless otherwise specified)

Model	ADC1140
RESOLUTION	16 Bits
CONVERSION TIME	35μs max
ACCURACY[1]	
Nonlinearity Error	±0.003% FSR[2] max
Differential Nonlinearity Error	±0.003% FSR[2] max
STABILITY	
Differential Nonlinearity	±2ppm/°C max
Gain (with internal reference)	±12ppm/°C max
(without internal reference)	±4ppm/°C max
Unipolar Offset	±30μV/°C max
Bipolar Offset	±7ppm/°C max
POWER SUPPLY SENSITIVITY	±0.002% FSR/% V_S
ANALOG INPUT	
Voltage Ranges	
Bipolar	±5V, ±10V
Unipolar	0 to +5V, 0 to +10V
Input Resistance	
0 to +5V	2.5kΩ
0 to +10V, ±5V	5.0kΩ
±10V	10.0kΩ
External Reference Input[3]	
Voltage Range	0 to +12V
Input Resistance	2.5kΩ
DIGITAL INPUT	
Convert Command	Positive Pulse, 100ns Width min Negative Edge Triggered
Logic Loading	1TTL Load
DIGITAL OUTPUT	
Parallel Output Data	
Unipolar	Binary (BIN)
Bipolar	Offset Binary (OBIN) Two's Complement
Output Drive	1TTL Load
Status	Logic "1" During Conversion
Output Drive	1TTL Load
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%
External Load Current	
(Rated Performance)	2mA max
Temperature Stability	±8.5ppm/°C max
POWER REQUIREMENTS[4]	
Voltage (Rated Performance)	±15V ±3%, +5V ±3%
Voltage (Operating)	±12V to ±17V, +4.75V to +5.25V
Supply Current Drain ±15V	±25mA
+5V	150mA
TEMPERATURE RANGE	
Specified	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +85°C
SIZE	2" X 2" X 0.4" (51 X 51 X 10.4mm)
Weight	1.2 oz (33g)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.

MATING CONNECTORS

AC1577 (2 REQUIRED)

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V	32	+15V
2	DIGITAL GROUND	31	-15V
3	MSB	30	ANALOG GROUND
4	MSB	29	ANALOG IN 1
5	BIT 2	28	ANALOG IN 2
6	BIT 3	27	ANALOG IN 3
7	BIT 4	26	+10V REF OUT
8	BIT 5	25	REFERENCE IN
9	BIT 6	24	OFFSET ADJUST
10	BIT 7	23	NOT USED
11	BIT 8	22	STATUS
12	BIT 9	21	CONVERT COMMAND
13	BIT 10	20	NOT USED
14	BIT 11	19	LSB
15	BIT 12	18	BIT 15
16	BIT 13	17	BIT 14

OTHER HIGH RESOLUTION PRODUCTS FROM ANALOG DEVICES:

- 14-Bit/15-Bit Sampling A/D Converters; DAS1152/53
  - 25kHz (14-Bit)/20kHz (15-Bit) throughput rates
  - Second Source to A/D/A/M824 and A/D/A/M825 Modules
- 14-Bit/15-Bit Low Level Data Acquisition Systems: DAS1155/56
  - 25kHz (14-Bit)/20kHz (15-Bit) throughput rates
  - High Performance PGIA (1V/V–1000V/V), SHA and A/D Converter
- 14-Bit Sample-Hold Amplifier: SHA1144
  - Acquisition Time: 8μs max to ±0.003% (20V step)

NOTES

[1] Offset and gain error are adjustable to zero by means of external potentiometers. See Figure 3 for proper connection.

[2] FSR means Full Scale Range.

[3] Rated performance is specified with +10.0V reference.

[4] Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

OPERATION

For operation, the only connections to the ADC1140 that are necessary are the power supplies, internal or external reference, input voltage pin programming, convert command and digital output. Refer to Table I for input pin programming and Figure 3 for offset and gain calibration.

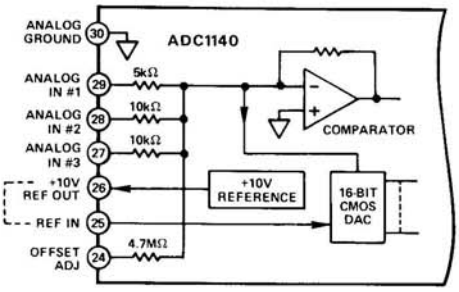


Figure 2. Analog Input Block Diagram

ANALOG INPUT PROGRAMMING

The analog input section consists of three analog input terminals. Analog input range selection is accomplished by pin programming as shown in Table I.

In the unipolar mode, a 0 to +10V or a 0 to +5V input signal develops a 0 to +2mA current that is compared to the 0 to −2mA (shown in Figure 2) current output of the DAC.

In the bipolar mode, a +1mA offset current from the reference is applied to the comparator input via pin programming connections. The ADC1140 can then accept either ±5V or ±10V inputs. These inputs again will be converted to current and compared with the DAC's 0 to −2mA current output.

Input Signal Range	Coding	Connect Input Signal To Pin(s)	Connect Pin 26 To Pin*	Connect Pin 30 To Pin(s)
±10V	OBIN, Two's Comp	28	27	29, 2
±5V	OBIN, Two's Comp	29	27	28, 2
0 to +5V	BIN	27, 28, 29	Open	2
0 to +10V	BIN	27, 28	Open	29, 2

*If Internal Reference is used, Pins 25 and 26 must be connected together through a 50Ω potentiometer or 24.9Ω fixed resistor (see Figure 3 and the gain calibration section).

Table I. Analog Input Voltage Pin Programming

OPTION OFFSET & GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 3. Proper offset and gain calibration requires great care and the use of an accurate and stable voltage reference. The voltage standard used as a signal source must be very stable. It should be capable of being set to within 1μV of the desired value at both ends of its range. The potentiometers selected should be of the good quality Cermet type. Multi-turn potentiometers having ten to fifteen turns and 100ppm/°C temperature coefficients will be adequate. The temperature coefficients contributed by these Cermet potentiometers will be less than 0.1ppm/°C.

By adjusting the offset first, gain and offset adjustments will remain independent of each other.

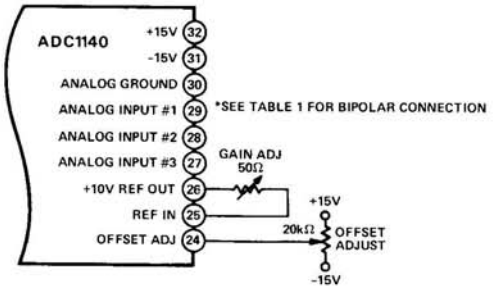


Figure 3. Offset and Gain Calibration

OFFSET CALIBRATION

For 0 to +10V range, set the input voltage precisely to +76μV; for 0 to +5V range, set it at +38μV. Adjust the zero potentiometer until the binary coded converter is just on the verge of switching from 000 . . . 00 to 000 . . . 01.

For ±5V range, set the input voltage precisely to −4.999924V; for ±10V range, set it at −9.999847V. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000 . . . 00 to 000 . . . 01 and the two's comp. coded units are just on the verge of switching from 100 . . . 0 to 100 . . . 1.

GAIN CALIBRATION

Set the input voltage precisely at +9.99977V for 0 to +10V input range, +4.99977V for ±5V input range, +9.99954V for ±10V input range, or +4.99988V for 0 to +5V input range, adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 111 . . . 0 to 111 . . . 1 and two's comp. coded units are just on the verge of switching from 011 . . . 10 to 011 . . . 11. Note that these values are 1 1/2 LSBs less than nominal full scale.

POWER SUPPLY AND GROUNDING CONNECTIONS

The analog power ground (pin 30) and digital ground (pin 2) are not connected internally. The connection must be made externally. The choice of an optimum "star" point is an important consideration in avoiding ground loops and to minimize coupling between the analog and digital sections. One suggested approach is shown in Figure 4.

Because the ADC1140 contains high quality tantalum capacitors on each of the power supply inputs to ground, external bypass capacitors are not required.

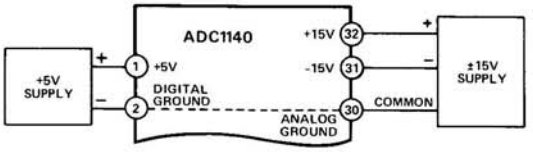


Figure 4. Power Supply and Grounding Techniques

ADC1140 TIMING

Conversion is initiated with the negative going edge of the Convert Command pulse as shown in Figure 5. The Convert Command pulse width must be a minimum of 100ns. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With the negative edge of the Convert Command pulse, all internal logic is reset. The MSB is set low with the remaining digitial outputs set to logic high state, and the status line is set high and remains high thru the full conversion cycle.

During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 16-bit conversion taking 35μs maximum. At this time, the STATUS line goes low signifying that the low conversion is complete.

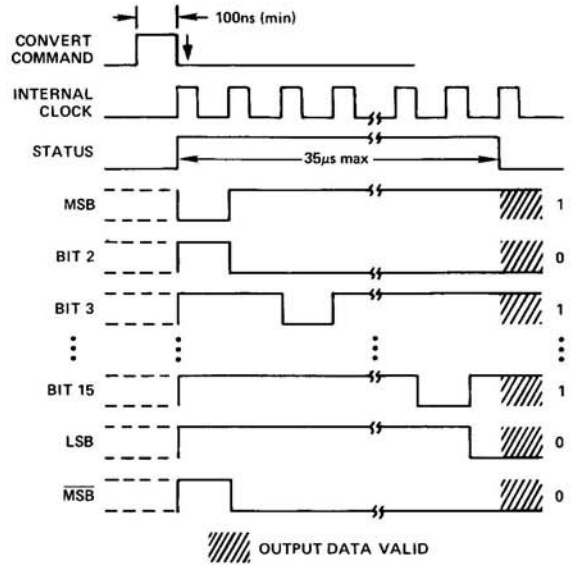


Figure 5. ADC1140 Timing Diagram

ANALOG INPUT/OUTPUT RELATIONSHIPS

The ADC1140 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is displayed on pin 4 for the binary and offset binary codes or on pin 3 for the two's complement code. Table II shows the unipolar analog input/digital output relationships. Table III shows the bipolar analog input/digital output relationships for offset binary code and two's complement codes.

Analog Input		Digital Output
0 to +5V Range	0 to +10V Range	Binary Code
+4.999924V	+9.99985V	1111 1111 1111 1111
+2.50000V	+5.00000V	1000 0000 0000 0000
+1.25000V	+2.50000V	0100 0000 0000 0000
+0.62500V	+1.25000V	0010 0000 0000 0000
+0.000076V	+0.000153V	0000 0000 0000 0001
+0.00000V	+0.00000V	0000 0000 0000 0000

Table II. Unipolar Input/Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	2's Complement Code
+4.99985V	+9.99970V	1111 1111 1111 1111	0111 1111 1111 1111
+2.50000V	+5.00000V	1100 0000 0000 0000	0100 0000 0000 0000
+0.000153V	+0.000305V	1000 0000 0000 0001	0000 0000 0000 0001
+0.00000V	+0.00000V	1000 0000 0000 0000	0000 0000 0000 0000
-5.00000V	-10.00000V	0000 0000 0000 0000	1000 0000 0000 0000

Table III. Bipolar Input/Output Relationships

HIGH RESOLUTION DATA ACQUISITION SYSTEM

Shown in Figure 6 is a high resolution data acquisition system. Here the SHA1144, a high resolution sample-hold amplifier, is used to drive the ADC1140. Conversion is initiated by the negative edge of the convert command pulse. At this time the STATUS pulse goes low causing the SHA1144 to go from the sample mode to the hold mode. When the conversion is complete, 35μs later, the STATUS pulse goes low, thus placing the SHA1144 in the sample mode.

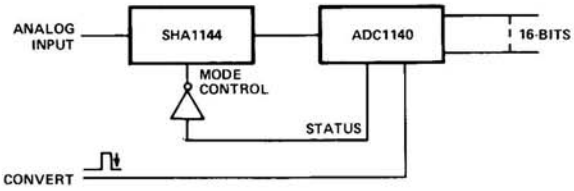


Figure 6. High Resolution Data Acquisition System

EXTERNAL REFERENCE

The ADC1140 is capable of operating with an external +10.0V reference. Simply disconnect the gain trim potentiometer from pin 26 and connect it to the external reference as shown in Figure 7. The external reference output must appear as a low impedance and must remain very stable during conversion to insure that accuracy is maintained. Gain error is adjusted as previously discussed in the gain calibration section.

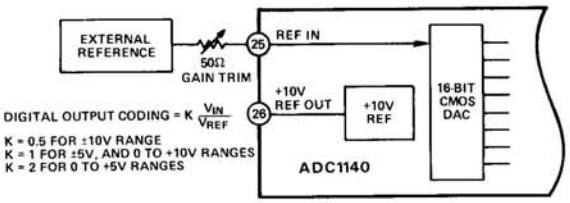


Figure 7. External Reference

The ADC1140 is factory tested and calibrated with the internal +10.0V reference voltage but nonstandard external voltages can be used with the digital output coding being determined by the formula shown in Figure 7.

PIA INTERFACE

The ADC1140 can be used with a PIA to interface directly to a microprocessor. As shown in Figure 8 the 16-bit output of the ADC1140 is split into two 8-bit bytes. Part A of the PIA is programmed to read the eight most-significant-bits while Part B reads the eight least-significant-bits. Output CB2 is used to start the ADC1140 conversion process. CB1, of the PIA, is used to sense the STATUS of the ADC1140 so that the end of conversions can be determined. The control bus, address bus, and data bus are then connected directly to the microprocessor.

With the use of PIAs, control of one or more ADC1140s can be accomplished in many different configurations.

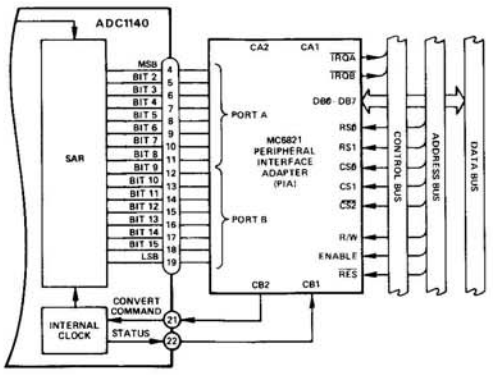


Figure 8. ADC1140 Interface to PIA

Intronics Power ®

Low Power/High Performance 16-Bit A/D Converter

ADC1143

FEATURES

Low Power Consumption:
- 175mW max, V_S = ±15V
- 150mW max, V_S = ±12V

Guaranteed Nonlinearity:
- ±0.006% FSR max (ADC1143J)
- ±0.003% FSR max (ADC1143K)

Guaranteed Differential Nonlinearity:
- ±0.006% FSR max (ADC1143J)
- ±0.003% FSR max (ADC1143K)

Low Differential Nonlinearity T.C.:
- ±2ppm/°C max (ADC1143J)
- ±1ppm/°C max (ADC1143K)

Fast Conversion Time:
- 70µs max (ADC1143J)
- 100µs max (ADC1143K)

Wide Power Supply Operation:
- V_S = ±11.4V to ±18.0V
- V_D = +3.0V to +18.0V

APPLICATIONS

Seismic Data Acquisition
Oil Well Instrumentation
Portable Industrial Scales
Portable Test Equipment
Robotics

GENERAL DESCRIPTION

The ADC1143 is a low power 16-bit successive-approximation analog-to-digital converter with a maximum power consumption of 175mW at V_S = ±15V, 150mW at V_S = ±12V, and is contained in a 2" × 2" × 0.4" module.

High performance like integral nonlinearity of ±0.006% FSR (ADC1143J)/ ±0.003% FSR (ADC1143K) and differential nonlinearity of ±0.006% FSR (ADC1143J)/ ±0.003% FSR (ADC1143K) are guaranteed. Additional guaranteed performance includes: differential nonlinearity T.C. of ±2ppm/°C (ADC1143J)/ ±1ppm/°C (ADC1143K), offset T.C. ±40µV/°C and gain T.C. ±12ppm/°C.

The ADC1143 makes extensive use of CMOS integrated circuits and thin-film components to obtain low power consumption, excellent performance and small size. The internal 16-bit CMOS DAC incorporates Analog Devices' proprietary thin-film resistor technology and proprietary current steering switches. CMOS successive-approximation registers, low power comparator and low noise reference are also used to optimize the performance of the ADC1143 (shown in Figure 1).

The ADC1143 can operate with power supply voltages ranging from ±11.4V dc to ±18.0V dc for V_S and +3V dc to +18V dc for the V_D supply. An internal voltage reference is provided, but an external reference can be used. Five analog input voltage ranges are selectable via user pin programming: +5V, +10V, +20V, ±5V and ±10V. Digital output coding in unipolar operation is true binary; for bipolar operation, the coding is offset binary or two's complement. Digital outputs are provided in both parallel and serial formats.

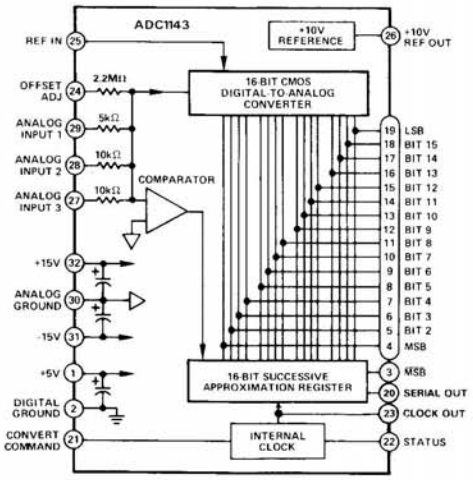


Figure 1. ADC1143 Functional Block Diagram

1400 PROVIDENCE HIGHWAY • BUILDING 2 NORWOOD, MASSACHUSETTS 02062-5015
PHONE: 781-551-5500 FAX: 781-551-5555

SPECIFICATIONS (typical @ +25°C, $V_S = \pm 15V$, $V_D = +5V$, $V_{REF} = +10V$ unless otherwise specified)

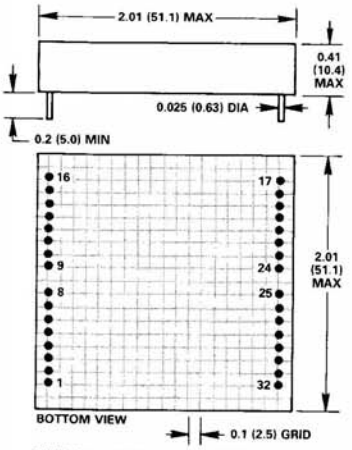
MODEL	ADC1143J	ADC1143K
RESOLUTION	16 Bits	*
CONVERSION TIME	70µs (max)	100µs (max)
ACCURACY		
Integral Nonlinearity	± 0.006% FSR[1] (max)	± 0.003% FSR[1] (max)
Differential Nonlinearity	± 0.006% FSR[1] (max)	± 0.003% FSR[1] (max)
No Missing Codes (0 to + 50°C)		
13 Bits	Guaranteed	
14 Bits		Guaranteed
STABILITY		
Differential Nonlinearity	± 2ppm/°C (max)	± 1ppm/°C (max)
Offset	± 40µV/°C (max)	*
Bipolar Offset	± 9ppm/°C (max)	*
Gain	± 12ppm/°C (max)	*
ANALOG INPUT		
Voltage Range		
Unipolar	+ 5V, + 10V, + 20V	*
Bipolar	± 5V, ± 10V	*
Input Resistance		
+ 5V	2.5kΩ	*
+ 10V, ± 5V	5.0kΩ	*
+ 20V, ± 10V	10.0kΩ	*
External Reference Input		
Voltage Range[2]	0 to + 12V	*
Input Resistance	10kΩ	*
DIGITAL INPUTS		
Convert Command	Positive Pulse, 1µs width (min) negative edge triggered	*
Logic Loading	CMOS Compatible	*
DIGITAL OUTPUTS		
Parallel Output Data		
Unipolar	Binary (BIN)	*
Bipolar	Offset Binary (OBIN), Two's Comp	*
Output Drive	CMOS Comp, 2LSTTL Loads	*
Status	"0" During Conversion	*
Output Drive	CMOS Comp, 2LSTTL Loads	*
Serial Output		
Output Drive	CMOS Comp, 1 LSTTL Load[3]	*
Clock Output		
Output Drive	CMOS Comp, 1 LSTTL Load	*
INTERNAL REFERENCE (V_{REF})		
Voltage	+ 10V, ± 0.3%	*
External Load Current	2mA max	*
Temperature Stability	± 8.5ppm/°C max	*
POWER REQUIREMENTS		
Voltage (rated performance)	± 15V(± 5%), + 5V(± 5%)	*
Voltage (operating)	± 11.4V to ± 18V, + 3V to + 18V	*
Supply Current Drain		
$+V_S = +15V$	4mA	*
$-V_S = -15V$	5mA	*
$+V_D = +5V$	4mA	*
Total Power		
$V_S = \pm 12V, V_D = +5V$	150mW max	*
$V_S = \pm 15V, V_D = +5V$	175mW max	*
POWER SUPPLY SENSITIVITY		
Offset	± 0.001%FSR/% $\pm V_S$	*
Gain	± 0.001%FSR/% $\pm V_S$	*
TEMPERATURE RANGE		
Rated Performance	0 to + 70°C	*
Operating	− 25°C to + 85°C	*
Storage	− 25°C to + 85°C	*
Relative Humidity	Meets MIL-STD 202E, Method 103B	*
SIZE	2" × 2" × 0.4" (50.8 × 50.8 × 10.16mm)	*
Weight	33g	*
PRICE		
(1–9)	$199	$229
(100-249)	$149	$172

NOTES:
[1]FSR Means Full Scale Range.
[2]Rated performance is specified with + 10.0V reference.
[3]LSTTL drive requires 2.2kΩ pulldown resistor.

Offset and gain errors are adjustable to zero by means of external potentiometers. See Figure 3 for proper connections.
Recommend Power Supply: Analog Devices Model 923
*Specifications same as ADC1143J
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.

MATING CONNECTORS AC1584-3 (2 REQUIRED) PRICE (1-9) $10

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V	32	+15V
2	DIGITAL GROUND	31	-15V
3	MSB	30	ANALOG GROUND
4	MSB	29	ANALOG IN 1
5	BIT 2	28	ANALOG IN 2
6	BIT 3	27	ANALOG IN 3
7	BIT 4	26	+10V REF OUT
8	BIT 5	25	REFERENCE IN
9	BIT 6	24	OFFSET ADJUST
10	BIT 7	23	CLOCK OUT
11	BIT 8	22	STATUS
12	BIT 9	21	CONVERT COMMAND
13	BIT 10	20	SERIAL OUT
14	BIT 11	19	LSB
15	BIT 12	18	BIT 15
16	BIT 13	17	BIT 14

OPERATION

For operation, the only connections to the ADC1143 that are necessary are the power supplies, internal or external reference, input voltage pin programming, convert command and digital output. Refer to Table I for input pin programming and Figure 3 for offset and gain calibration.

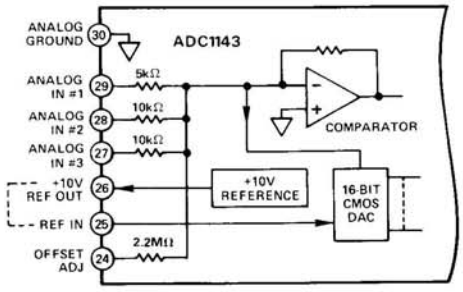


Figure 2. Analog Input Block Diagram

ANALOG INPUT RANGE

The analog input voltage section of the ADC1143 consists of three analog input terminals (see Figure 2). Analog input voltage range selection is accomplished by pin programming as shown in Table I.

In the unipolar mode, a +5V, +10V or +20V input signal can be applied. These input voltages develop a 0 to +2mA current which is compared to the 0 to −2mA current output of the internal reference DAC in the ADC1143. In the bipolar mode, a ±5V or ±10V input signal can be applied. These input voltages develop a ±1mA current which is compared to a 0 to −2mA current of the internal reference DAC which is offset by +1mA, to produce a ±1mA current.

OFFSET AND GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 3. Proper offset and gain calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage reference used as a signal source must be very stable and have the capability of being set within ±1μV of the desired value. The potentiometers should be good quality cermet type. Multiturn potentiometers having ten to fifteen turns and ±100ppm/°C temperature coefficients will be adequate. The temperature coefficient contribution will be less than ±0.1ppm/°C.

By adjusting the offset first, gain and offset adjustment will remain independent of each other.

OFFSET CALIBRATION

For +5V range, set the input voltage to precisely +38μV; for +10V range, set it to +76μV; for +20V range, set it to +153μV.

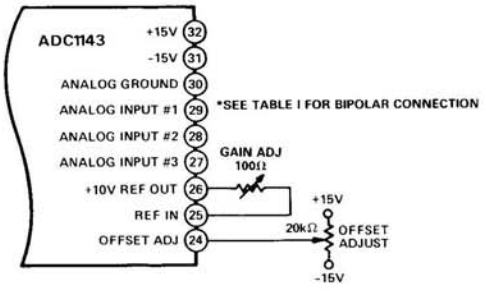


Figure 3. Offset and Gain Calibration

Adjust the offset potentiometer until the binary output code is on the verge of switching from 000 . . . 00 to 000 . . . 01.

For ±5V range, set the input voltage to precisely −4.999924V; for ±10V range, set it to −9.999847V. Adjust the offset potentiometer until the offset binary code is on the verge of switching between 000 . . . 00 and 000 . . . 01, and two's complement coded units are switching from 100 . . . 00 to 100 . . . 01.

GAIN CALIBRATION

For +5V range, set the input voltage to precisely +4.99988V; for +10V range, set it to +9.99977V; for +20V range, set it to +19.9995V. Adjust the gain potentiometer until the binary output code is on the verge of switching from 111 . . . 10 to 111 . . . 11.

For ±5V range, set the input voltage to precisely +4.99977V; for ±10V range, set it to +9.99954V. Adjust the gain potentiometer until the offset binary code is on the verge of switching from 111 . . . 10 to 111 . . . 11, and the two's complement coded units are switching from 011 . . . 10 to 011 . . . 11.

POWER SUPPLY AND GROUNDING CONNECTIONS

The analog power ground (pin 30) and digital ground (pin 2) are not connected internally in the ADC1143, thus the connection must be made externally. The choice of an optimum "star" point is an important consideration in avoiding ground loops and to minimize coupling between the analog and digital sections. One suggested approach is shown in Figure 4.

Because the ADC1143 contains high quality tantalum capacitors on each of the power supply inputs to ground, external bypass capacitors are not required.

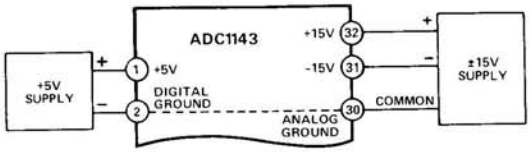


Figure 4. Power Supply and Grounding Techniques

Input Voltage Range	Output Coding	Connect Input Signal To Pin(s)	Connect Pin* 26 to Pin #	Connect Pin 30 to Pin(s)
+5V	BIN	27, 28, 29	open	2
+10V	BIN	27, 28	open	2, 29
+20V	BIN	27	open	2, 28, 29
±5V	OBIN, 2's Comp	29	27	2, 28
±10V	OBIN, 2's Comp	28	27	2, 29

*If internal reference is used, Pins 25 and 26 must be connected together through a 100Ω potentiometer or 49.9Ω fixed resistor (see Figure 3 and Gain Calibration Section).

Table I. Analog Input Voltage Range Pin Programming

EXTERNAL REFERENCE

The ADC1143 is capable of operating with an external reference. Simply disconnect the gain trim potentiometer from Pin 26 and connect it to the external reference as shown in Figure 5. The ADC1143 is tested and specified with a +10.0V reference. An external reference with a voltage of 0 to +12V can be applied. The external reference must appear as a low impedance and must remain very stable during conversion to insure that accuracy is maintained.

When using an external reference, the digital output coding can be determined by the formula shown in Figure 5.

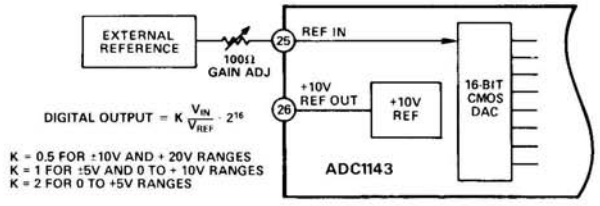


Figure 5. External Reference

ADC1143 TIMING

Conversion is initiated with the negative going edge of the convert command pulse as shown in Figure 6. The convert command pulse width must be a minimum of 1μs. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With the negative edge of the convert command pulse, all internal logic is reset. The MSB is set high with the remaining bits set to logic low. The status line is set low and remains low through the full conversion cycle.

During conversion, each bit starting with the MSB is set high on the rising edge of the internal clock. The ADC's internal DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete conversion of the ADC1143J and ADC1143K

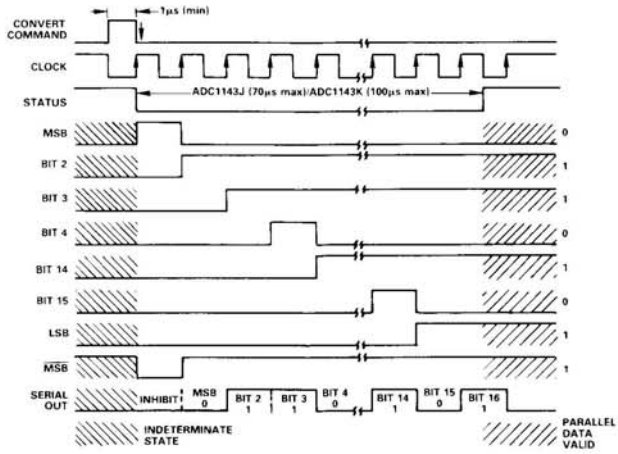


Figure 6. ADC1143 Timing Diagram

taking 70μs max and 100μs max respectively. The parallel output data is valid on the rising edge of the status line.

Serial output data is valid for each bit at the completion of clock cycle used to make the bit decision as shown in Figure 6.

SEISMIC DATA ACQUISITION APPLICATION

The ADC1143's low power consumption and high performance make it ideally suited for portable seismic data acquisition systems like the one shown in Figure 7. In seismic data acquisition systems, geophones are used to receive reflected shock waves from subsurface strata, induced by controlled discharge of explosives. These reflected signals may travel several miles before reaching the geophones and are difficult to discern from noise or other interference like ground roll. The low level signals from the geophones are amplified and filtered appropriately to remove the undesired signals. The conditioned signal is amplified by the PGA then held by SHA and converted to digital form by the ADC1143. The digital data is stored on an on-site recorder for later data collection and processing.

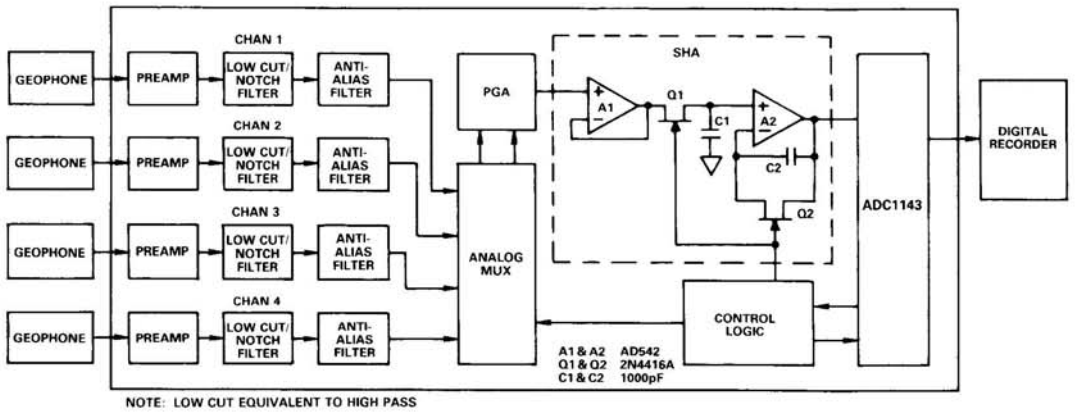


Figure 7. Seismic Data Acquisition System Block Diagram

Intronics Power ®

High Resolution 16- and 18-Bit Digital-to-Analog Converters

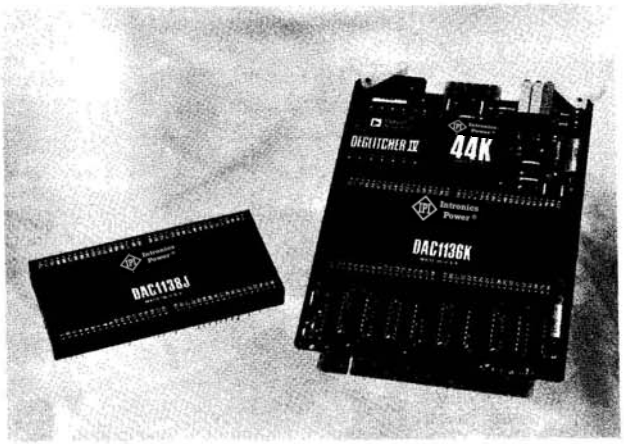
DAC1136/1138

FEATURES

DAC1138
- 18-Bit Resolution and Accuracy (38μV, 1 Part in 262,144)
- Nonlinearity 1/2LSB max (DAC1138K)
- Excellent Stability
- Settling to 1/2LSB (0.0002%) in 10μs
- Hermetically-Sealed Semiconductors

DAC1136
- 16-Bit Resolution and Accuracy (152μV, 1 Part in 65,536)
- Low Cost
- Nonlinearity 1/2LSB max (DAC1136K, L)
- Settling to 1/2LSB max (0.0008%) in 6μs

DEGLITCHER IV
- Eliminates DAC Glitches
- Available on DAC1136/1138 Card-Mounted Assembly



GENERAL DESCRIPTION

The DAC1136/1138 are complete self-contained current or voltage output modular digital-to-analog converters with resolutions and accuracies of 16 and 18 bits.

The DAC1136/1138 combine precision current sources with state-of-the-art steering switches to produce a very linear output. Inputs to these converters are compatible with TTL levels. The converters have a current output of −2mA full scale. A voltage output can be obtained by connecting the internal amplifier to the current output by means of jumpers. By using additional jumpers, the user can select any one of the following output ranges: 0 to +5V, 0 to +10V, ±5V, or ±10V.

The DAC1136/1138 are available on Card-Mounted Assemblies. In this configuration, selectable options include: input codes, output amplifiers, and a high speed transient-suppressing Deglitcher Module, Deglitcher IV.

WHERE TO USE HIGH RESOLUTION DACS

The DAC1136/1138 deliver exceptional accuracy for a broad range of display, test and instrumentation applications. The DAC1136, with a resolution of 16 bits or 1 part in 65,536, and the DAC1138 with a resolution of 18 bits or 1 part in 262,144 are ideally suited for applications requiring wide dynamic range measurement and control. Applications include data acquisition systems, high resolution CRT displays, automatic semiconductor testing, photo-typesetting, frequency synthesis and nuclear reactor control.

CERTIFICATE OF CALIBRATION

Each DAC1138 has been calibrated with equipment and methods that are traceable to the National Bureau of Standards (NBS). A Certificate of Performance is sent with each unit, which includes linearity test data.

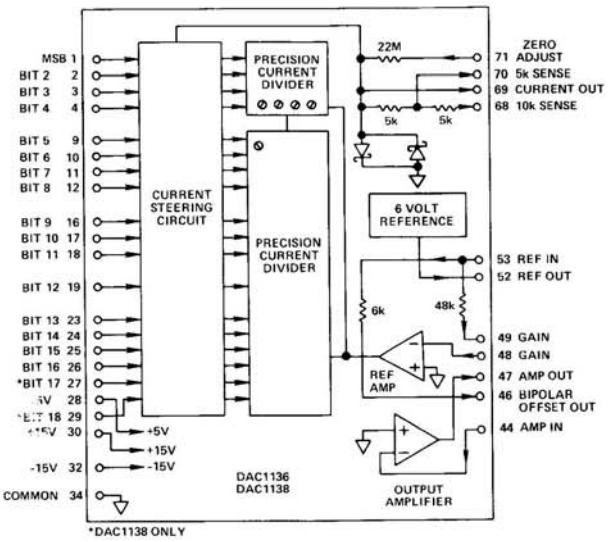


Figure 1. Block Diagram and Pin Designations

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PHONE: 781-551-5500 FAX: 781-551-5555

SPECIFICATIONS (typical @ +25°C, rated power supplies unless otherwise noted; specifications for mounting card with amplifier/deglitcher options same as module unless otherwise noted)

	DAC1136 Module			DAC1136 on Mounting Card with Amplifier/Deglitcher Options.		
	J	K	L	Deglitcher IV (Internal AD542K)	Low Drift 234L w/wo Deglitcher	High Speed 44K w/wo Deglitcher
RESOLUTION, BITS	16					
ACCURACY						
Integral Nonlinearity	±1LSB max	±1/2LSB max	±1/2LSB max			
Differential Nonlinearity	±1LSB max	±1/2LSB max	±1/2LSB max			
Gain and Offset Error (Externally Adjustable)				Gain, offset and glitch–nulling adjustments provided on the mounting card.		
ANALOG OUTPUT						
Unipolar Mode	−2mA to 0mA					
Bipolar Mode	−1mA to +1mA					
Voltage Output Range (Pin Selectable)	0 to +5V, 0 to +10V, ±5V, ±10V					
DIGITAL INPUTS	TTL/CMOS; See Figure 2					
INPUT CODES						
Unipolar Mode	Complementary Binary (COMP BIN)			BIN, COMP BIN, 2's COMP, COMP 2's COMP		
Bipolar Mode	Complementary Offset Binary (COMP OBIN)			OBIN, COMP OBIN SIGN PLUS MAG BIN, COMP SIGN PLUS MAG BIN		
STROBE INPUT	None			One standard series 74LS load, leading-edge triggered, pulse width 100ns minimum.		
DYNAMIC CHARACTERISTICS						
Settling Time to 1/2LSB						
Current						
Full Scale Step	8µs			Voltage Output, Only		
LSB Step	6µs			Voltage Output, Only		
Voltage						
Unipolar (10V Step)	90µs			80µs	45µs	25µs
Bipolar (20V Step)	250µs			90µs	60µs	30µs
LSB Step	8µs			8µs	8µs	8µs
Slew Rate	1V/µs			2V/µs	6V/µs	20V/µs
TEMPERATURE COEFFICIENTS (ppm of FSR/°C)[1]						
Integral Nonlinearity	±1	±1	±1.5 max			
Differential Nonlinearity	±1	±1	±1.5 max			
Gain (Excluding V_{REF})	±5	±5	±8 max			
Offset						
Unipolar Mode	±0.5			±0.5	±0.1	±2
Bipolar Mode	±5					
STABILITY, LONG TERM (ppm of FSR/1,000 hrs.)[2]						
Gain (Excluding V_{REF})	±5					
Offset	±6			±1	±0.5	±25
NOISE (Include V_{REF}; Double for Bipolar Mode)						
Output Current (BW = 100kHz)	0.5nA rms			Voltage Output, Only		
Output Voltage (BW = 0.1–10Hz)						
@ 0V (All 1's Code; "ZERO")	4µV pk-pk					
@ 5V (MSB = 0 Code; "Half Scale")	6µV pk-pk					
@ 10V (All 0's Code; "Full Scale")	9µV pk-pk					
Output Voltage (BW = 100kHz)	30µV rms			20µV rms	40µV rms	35µV rms
VOLTAGE COMPLIANCE (Amplifier Offset, E_{OS})						
Max E_{OS} Allowed for Rated Accuracy	±2mV max					
Initial E_{OS} (Factory Adj.)	±100µV			±50µV	±20µV	±100µV
E_{OS} Drift	±10µV/°C			±5µV/°C	±0.1µV/°C	±15µV/°C
Current Output (pin 69)						
Voltage Protection	via Internal Schottky Diodes					
Source Resistance						
Unipolar Mode	>33kΩ					
Bipolar Mode	>5kΩ					
Source Capacitance	150pF					
REFERENCE VOLTAGE (V_{REF})						
Voltage (Z_{OUT} ≈ 200Ω)	+6.000V (Maximum Error, ±0.024V)					
Noise (BW = 0.1–10Hz)	3µV pk-pk					
Tempco	5ppm/°C					
POWER SUPPLY REQUIREMENTS[3]						
−5V dc, ±5%	9mA				95mA	
±15V dc, ±5%	±30mA			±38mA	±37mA	±40mA
POWER SUPPLY REJECTION (±15V dc)						
Gain or Offset vs. FSR	80dB			100dB	100dB	75dB
Differential Nonlinearity	±1/4LSB per Volt ΔV_S					
ENVIRONMENTAL						
Operating Temperature	0 to +70°C			−55°C to +85°C	−55°C to +85°C	−55°C to +85°C
Storage Temperature	−55°C to +85°C					
Humidity	5% to 95%, Noncondensing					

NOTES

[1]Maximum temperature coefficients guaranteed from 15°C to 35°C, typical from 0 to +70°C.

[2]Recommended DNL calibration check: 6 months.

[3]Recommended Power Supply: Analog Devices Model 923.

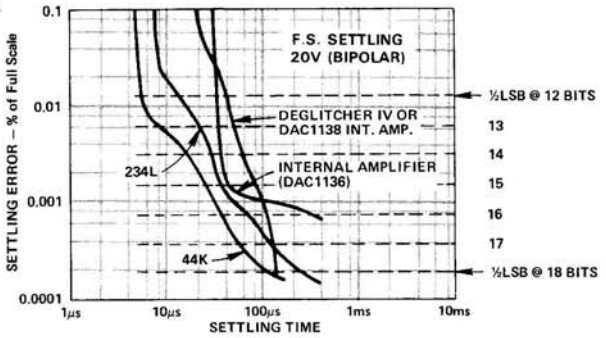
Specifications subject to change without notice.

SPECIFICATIONS (typical @ +25°C, rated power supplies unless otherwise noted; specifications for mounting card with amplifier/deglitcher options same as module unless otherwise noted)

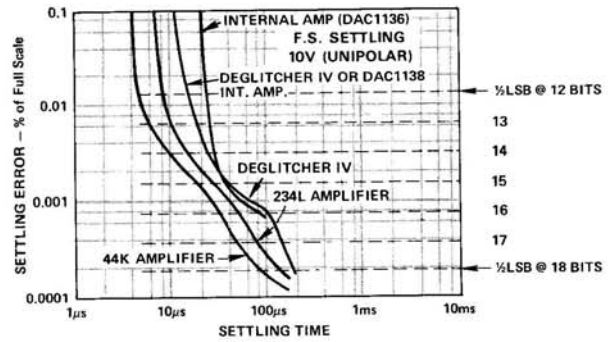
	DAC1138 Module		DAC1138 on Mounting Card with Amplifier/Deglitcher Options.	
	J	K	Deglitcher IV (Internal AD542K)	Low Drift 234L w/wo Deglitcher
RESOLUTION, BITS	18			
ACCURACY				
Integral Nonlinearity	±1LSB max	±1/2LSB max		
Differential Nonlinearity	±1LSB max	±1/2LSB max		
Gain and Offset Error (Externally Adjustable)			Gain, offset and glitch-nulling adjustments provided on the mounting card.	
ANALOG OUTPUT				
Unipolar Mode	−2mA to 0mA			
Bipolar Mode	−1mA to +1mA			
Voltage Output Range (Pin Selectable)	0 to +5V, 0 to +10V, ±5V, ±10V			
DIGITAL INPUTS	TTL/CMOS; See Figure 2			
INPUT CODES				
Unipolar Mode	Complementary Binary (COMP BIN)		BIN, COMP BIN, 2's COMP, COMP 2's COMP	
Bipolar Mode	Complementary Offset Binary (COMP OBIN)		OBIN, COMP OBIN SIGN PLUS MAG BIN, COMP SIGN PLUS MAG BIN	
STROBE INPUT	None		One standard series 74LS load, leading-edge triggered, pulse width 100ns minimum.	
DYNAMIC CHARACTERISTICS				
Settling Time to 1/2LSB				
Current				
Full Scale Step	10µs		Voltage Output, Only	
LSB Step	8µs		Voltage Output, Only	
Voltage				
Unipolar (10V Step)	175µs		80µs	45µs
Bipolar (20V Step)	140µs		90µs	60µs
LSB Step	18µs		18µs	18µs
Slew Rate	2V/µs		2V/µs	6V/µs
TEMPERATURE COEFFICIENTS (ppm of FSR/°C)				
Integral Nonlinearity	±0.3			
Differential Nonlinearity	±0.4			
Gain (Excluding V_{REF})	±0.8			
Offset				
Unipolar Mode	±0.5		±0.5	±0.1
Bipolar Mode	±1			
STABILITY, LONG TERM (ppm of FSR/1,000 hrs.)[1]				
Gain (Excluding V_{REF})	±2			
Offset	±2		±1	±0.5
NOISE (Include V_{REF}; Double for Bipolar Mode)				
Output Current (BW = 100kHz)	0.5nA rms		Voltage Output, Only	
Output Voltage (BW = 0.1–10Hz)				
@ 0V (A11 1's Code; "ZERO")	4µV pk-pk			
@ 5V (MSB = 0 Code; "Half Scale")	6µV pk-pk			
@ 10V (A11 0's Code; "Full Scale")	9µV pk-pk			
Output Voltage (BW = 100kHz)	30µV rms		20µV rms	40µV rms
VOLTAGE COMPLIANCE (Amplifier Offset, E_{OS})				
Max E_{OS} Allowed for				
Rated Accuracy	±200µV max			
Initial E_{OS} (Factory Adj.)	±100µV		±50µV	±20µV
E_{OS} Drift	±10µV/°C		±5µV/°C	±0.1µV/°C
Current Output (pin 69)				
Voltage Protection	via Internal Schottky Diodes			
Source Resistance				
Unipolar Mode	>33kΩ			
Bipolar Mode	>5kΩ			
Source Capacitance	150pF			
REFERENCE VOLTAGE (V_{REF})				
Voltage ($Z_{OUT} \approx 200\Omega$)	+6.000V (Maximum Error, ±0.024V)			
Noise (BW = 0.1–10Hz)	3µV pk-pk			
Tempco	5ppm/°C			
POWER SUPPLY REQUIREMENTS[2]				
+5V dc, ±5%	9mA			95mA
±15V dc, ±5%	±30mA		±38mA	±37mA
POWER SUPPLY REJECTION (±15V dc)				
Gain or Offset vs. FSR	80dB		100dB	75dB
Differential Nonlinearity	±1/4LSB per Volt ΔV_S			
ENVIRONMENTAL				
Operating Temperature	0 to +70°C			
Storage Temperature	−55°C to +85°C		−55°C to +85°C	−55°C to +85°C
Humidity	5% to 95%, Noncondensing			

NOTES:
[1]Recommended DNL calibration check: 6 months.
[2]Recommended Power Supply Analog Devices: Model 923.
Specifications subject to change without notice.

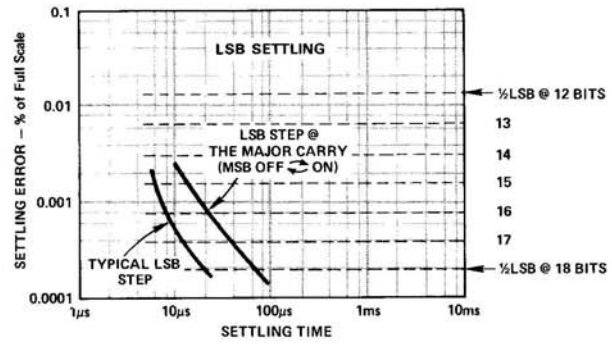
Characteristic Curves*



Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for 20V Output Step (+10V ⇄ -10V)



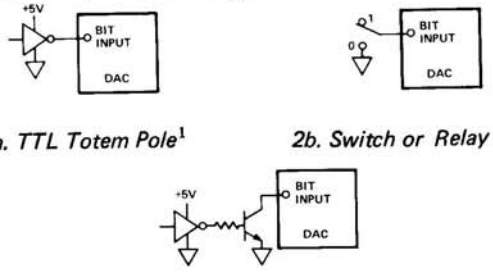
Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for 10V Output Step (0V ⇄ +10V)



Settling Time (Voltage Output) vs. %-of-Full-Scale-Error for LSB Steps (Essentially Independent of Amplifier Used). With Deglitcher IV, the LSB Step at the Major Carry Settles as Fast as the Typical LSB Step, Following the 11μs Hold Period.

INPUT CONSIDERATIONS

The DAC1136/1138 may be driven by TTL or CMOS as shown in Figure 2. Note that the TTL input is shown with inputs for both a direct "totem pole" TTL gate and open collector (or "pull-up") configurations.



2a. TTL Totem Pole[1] *2b. Switch or Relay Input[2]*

2c. CMOS Input

1. FOR TTL WITH OPEN COLLECTOR, DO NOT USE EXTERNAL PULL-UP. CONVERTERS HAVE INTERNAL 10kΩ PULL-UP ON EACH INPUT TO 3.8V.
2. USE SPST SWITCH OR RELAY TO GROUND. WHEN SWITCH IS OPEN, THE INTERNAL 10kΩ WILL PULL INPUT UP TO 3.8V.

Figure 2. Input Connections

OUTPUT CONNECTIONS AND GUARDING

The DAC1136/1138 output connections for various voltage ranges are shown in Figure 3.

Since an LSB is only 38μV (at 10 volts full scale for the DAC1138), care must be exercised to properly guard the current output of the converter from leakage current. Any connection made to the DAC's current output (pin 69) should be guarded. Suggested printed circuit board guarding is shown in Figure 3. The optional Card-Mounted Assemblies of the DAC1136/1138 have been carefully designed for optimum guarding and performance.

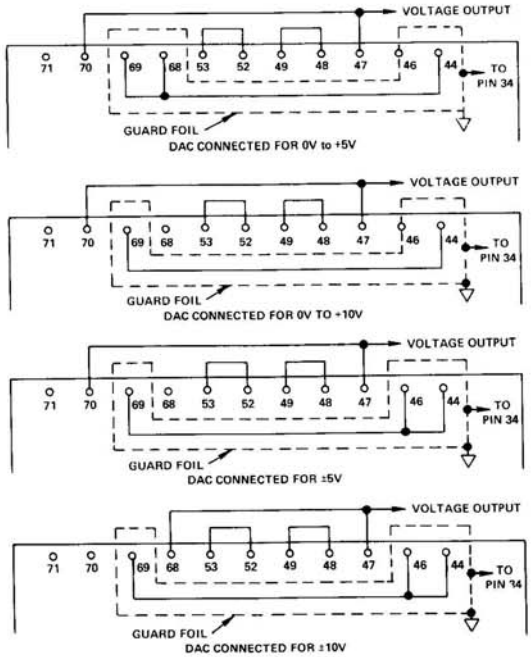
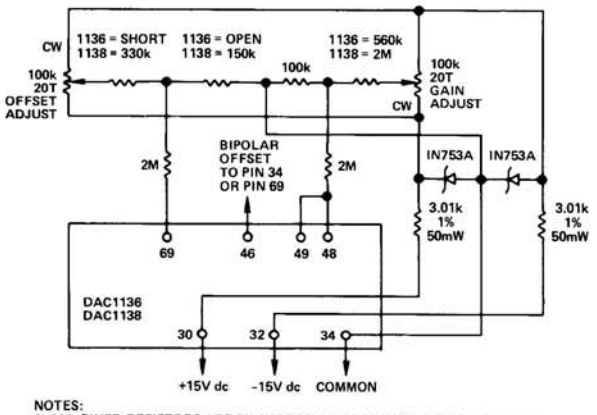


Figure 3. Output Voltage Connections and Suggested PCB Guarding (Unipolar and Bipolar)

*NOTE: All curves typical at rated supply voltage.
F.S. = Full Scale

GAIN AND OFFSET ADJUSTMENTS

The gain and offset adjustments are made with external potentiometers which the user supplies. With the appropriate digital inputs applied, these potentiometers are adjusted until the desired output voltage is obtained. The proper connections for offset and gain are shown in Figure 4. The voltmeter used to measure the output should be capable of stable resolution of 1/4LSB in the region of zero and full scale. Because of the interaction between offset and gain adjustments, the adjustment procedure described below should be carefully followed. Offset adjustment affects gain, but gain adjustment does not affect offset.



NOTES:
1. ALL FIXED RESISTORS ARE 5% CARBON COMP, UNLESS OTHERWISE NOTED.
2. ALL POTENTIOMETERS ARE 20-TURN INFINITE RESOLUTION TYPE.

Figure 4. Gain and Offset Adjustments

For unipolar mode, apply a digital input of all "1's" (complementary binary code for zero output) and adjust the offset potentiometer until a 0.00000V output is obtained (see Table I). Once the appropriate offset adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output is obtained (see Table I).

For bipolar mode, apply a digital input of all "1's" (complementary offset binary code for minus full scale) and adjust the offset potentiometer for the proper minus full scale output voltage (see Table I). Once the appropriate minus full scale adjustment has been made, apply a digital input of all "0's". Adjust the gain potentiometer until the plus full scale output shown below is obtained.

RANGE	IDEAL OUTPUT		
		DAC1138	DAC1136
Unipolar:	All 11...1	All 00...0	
0V→+10V	0.00000V	+9.999962V	+9.999848V
0V→+5V	0.00000V	+4.999981V	+4.999924V
Bipolar:			
-10V→+10V	-10.00000V	+9.999934V	+9.999695V
-5V → +5V	-5.00000V	+4.999962V	+4.999848V
To adjust:	Adjust ZERO pot	Adjust GAIN pot	

Table I. Full Scale Output

DIFFERENTIAL LINEARITY ADJUSTMENT

Each DAC1136/1138 has been factory calibrated and tested to achieve the performance indicated in the electrical specifications. Before attempting recalibration, it is imperative that the circuit be checked to confirm that all previously described precautions have been taken to insure proper application at the 16- or 18-bit level. Basically, the DAC is trimmed by comparing a bit to the sum of all lower bits, and adjusting, if necessary, for a one LSB positive difference. The top 4 major carries, i.e., MSB minus the sum of bits 2-through-the-LSB, down through bit 4 minus the sum of bits 5-through-the-LSB, can be trimmed using the procedure outlined below. A differential voltmeter capable of 100μV Full Scale should be connected to V_{OUT} of the DAC. This will resolve an LSB which at 18 bits is 38μV (10V range). A Fluke 895A or equivalent is recommended.

1. Bit 4 Trim
   a. Set bit inputs to 11110 . . . . 0.
   b. Read the output voltage by nulling the voltmeter.
   c. Set bit inputs to 11101 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 1b plus 1LSB. Adjust bit 4 if required (see B4, Figure 6).

2. Bit 3 Trim
   a. Set bit inputs to 1110 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set inputs to 1101 . . . . 1.
   d. Read voltage by nulling the voltmeter. This reading should be equal to that of step 2b plus 1LSB. Adjust bit 3 if required (see B3, Figure 6).

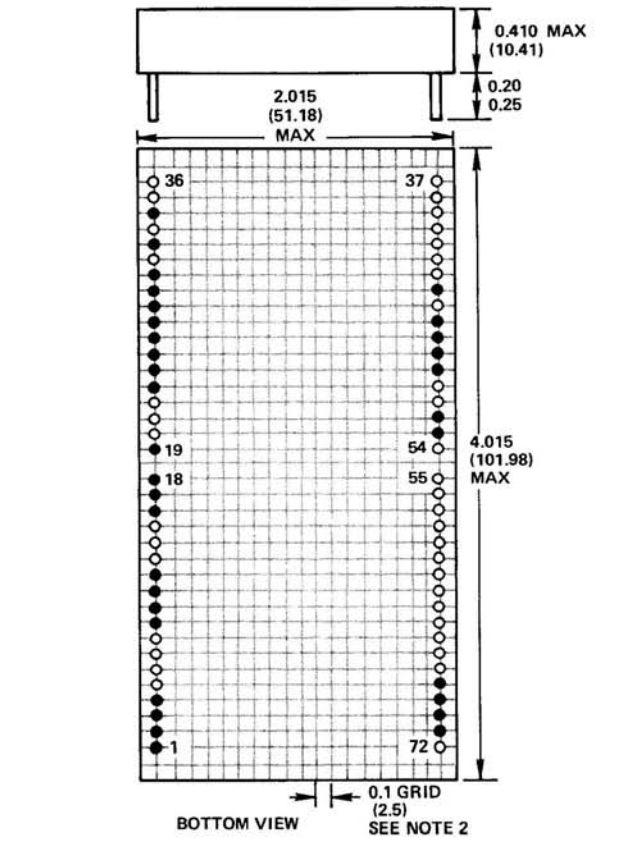
3. Bit 2 Trim
   a. Set bit inputs to 110 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set bit inputs to 101 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 3b plus 1LSB. Adjust bit 2 if required (see B2, Figure 6),

4. Bit 1 (MSB) Trim
   a. Set bit switches to 100 . . . . 0.
   b. Read output voltage by nulling the voltmeter.
   c. Set bit switches to 011 . . . . 1.
   d. Read voltage by nulling voltmeter. This reading should be equal to that of step 4b plus 1LSB. Adjust bit 1 (MSB) if required (see MSB, Figure 6).

If insufficient range exists on any adjustment, then a separate adjustment for the weight of bits 5-through-the-LSB (see Sum B5 → LSB, Figure 6) should be performed. This condition will probably not occur on bit 2, 3 and 4 but might occur on the MSB. If adjustment of the sum of bits 5-through-the-LSB is made, the trim procedure for all bits should be repeated. Obviously, since the procedure affects the weight of individual bits, it affects the overall gain of the DAC. The final step should be adjustment of gain (user supplied adjustment external to module, or pot at edge of mounting card).

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

Dimensions shown in inches and (mm).



NOTES:
1. PINS: 0.019 ±0.001 DIA.
2. GRID AND MARKINGS NEXT TO PINS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON UNIT.
3. PINS 27 AND 29 ARE NOT PRESENT ON DAC1136.

ASSEMBLY INSTRUCTIONS

CAUTION: This module is not an embedded assembly and is not hermetically sealed. Do not subject to a solvent or water-wash process that would allow direct contact with free liquids or vapors. Entrapment of contaminants may occur, causing performance degradation and permanent damage. Install after any clean/wash process and then only spot clean by hand.

USING AN EXTERNAL 6V REFERENCE

The DAC1136/1138 can be operated with an external reference connected to pin 53 of the module. The current drain on the external reference will be 1.125mA in bipolar mode or 0.125mA in unipolar mode (pin 46 should be left open and not grounded when using an external reference in the unipolar mode). When an external reference is used, pin 52, (the output of the internal reference) is left open.

Codi Semiconductor manufactures a reference module called Certavolt[1] with a 10 volt output accurate to 0.001%. This output is temperature compensated to within 1ppm/°C from +15°C to +55°C. The Certavolt requires a power supply of +28V dc @ 20mA. To convert the +10 volt output of the Certavolt to the +6 volt reguired by the DAC, the circuit shown in Figure 5 is recommended.

[1] Certavolt is a registered trade name by Codi Semiconductor.

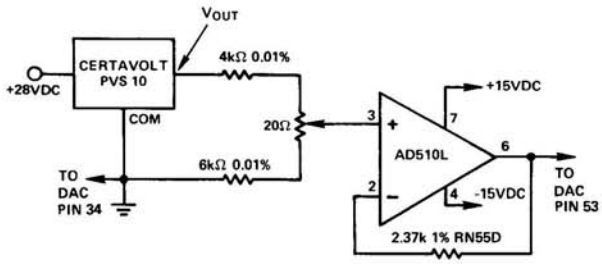
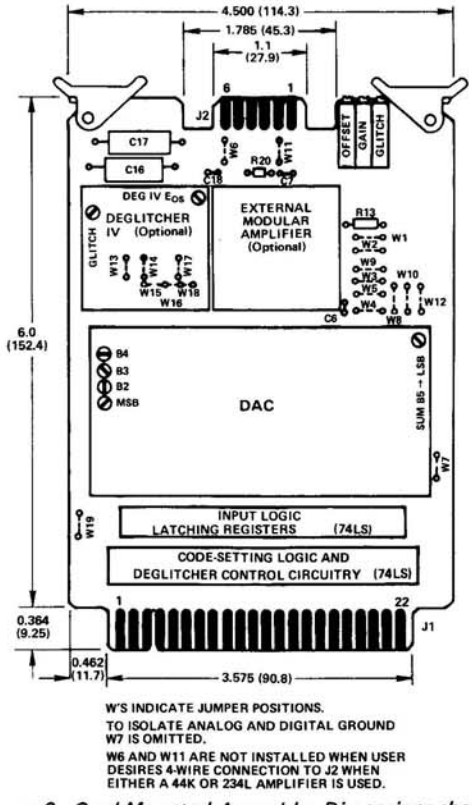


Figure 5. DAC1136/1138 with External Precision Reference

OPTIONAL CARD-MOUNTED ASSEMBLY

Analog Devices offers an optional Card-Mounted Assembly designed to provide optimum performance at the 18-bit level. As shown in Figure 6, this 4 1/2" X 6" printed circuit card includes the appropriate DAC GAIN and OFFSET adjustment potentiometers, power supply bypass capacitors and input registers. The Card-Mounted Assembly can be ordered with custom code-setting logic, external output amplifiers, and a Deglitcher IV.



W'S INDICATE JUMPER POSITIONS.
TO ISOLATE ANALOG AND DIGITAL GROUND W7 IS OMITTED.
W6 AND W11 ARE NOT INSTALLED WHEN USER DESIRES 4-WIRE CONNECTION TO J2 WHEN EITHER A 44K OR 234L AMPLIFIER IS USED.

Figure 6. Card-Mounted Assembly. Dimensions shown in inches and (mm).

CARD-MOUNTED ASSEMBLY JUMPER DESIGNATIONS

The output voltage range, reference source, amplifier and deglitcher configurations are programmed at the factory by means of jumpers, resistors, and capacitors (see ordering guide for details). The mounting card can be programmed by the user, if necessary, as shown below.

Output Voltage Range	Install Jumpers
±10V	W10, W5
±5V	W12, W5
+10V	W12, W3

Reference	Install Jumpers
Internal	W2
External	W1

Amplifier	Install Jumpers
Internal	W4, W9
External[1]	W8, W13
Deglitcher IV[2]	W8, W15, W17, W18
Deg. IV with Ext Amp[3]	W8, W14, W16

NOTES:

[1] With a 234L amplifier install C7 (0.01μF, 10%, ceramic capacitor). With a 44K amplifier use a variable resistor (typ value ≈ 499Ω, 0.1W, 1%) to adjust the output voltage for a ±100μV reading as measured between pins 69 and 34 of the DAC (this step sets voltage compliance); install this value resistor (R13 position).

[2] With Deglitcher IV remove R20 (100Ω) and replace the resistor with a jumper.

[3] With Deglitcher IV and a 234L amplifier remove C6 (6.8pF Capacitor) and install: C7 (0.01μF, 10%, ceramic capacitor), C18 (100pF, 10%, ceramic capacitor), C17 (1000pF, 10%, polystyrene capacitor) and replace R20 (100Ω) with a jumper. With Deglitcher IV and a 44K amplifier perform the operation described in Note 1, remove C6 (6.8pF capacitor) and install: C18 (100pF, 10%, ceramic capacitor), C17 (1000pF, 10% polystyrene capacitor) and replace R20 (100Ω) with a jumper.

CONNECTOR J1

PIN	FUNCTION	PIN	FUNCTION
A	BIT 1	U	STROBE
B	BIT 2	V	BIT 18[1]
C	BIT 3	W	+5V
D	BIT 4	X	+15V
E	BIT 5	Y	-15V
F	BIT 6	Z	DIGITAL GND
H	BIT 7	1-4	NC
J	BIT 8	5	INTERLOCK
K	BIT 9	6	INTERLOCK
L	BIT 10	7-16	NC
M	BIT 11	17	BIT 17[1]
N	BIT 12	18	
P	BIT 13	19	
R	BIT 14	20	
S	BIT 15	21	
T	BIT 16	22	

J1 MATES WITH CINCH P.N. 251-22-30-160 (SUPPLIED).

[1] DAC1138 ONLY

CONNECTOR J2

PIN	FUNCTION
1	ANALOG SENSE LOW
2	ANALOG SOURCE LOW
3	NC
4	ANALOG SOURCE HIGH
5	ANALOG SENSE HIGH
6	ANALOG REF. IN/OUT
A	ANALOG REF. IN/OUT
B	ANALOG SENSE HIGH
C	ANALOG SOURCE HIGH
D	NC
E	ANALOG SOURCE LOW
F	ANALOG SENSE LOW

J2 MATES WITH CINCH P.N. 251-06-30-160 (SUPPLIED).

Mounting Card Connector Designations

DEGLITCHER IV

The Deglitcher IV is a precision high-speed, high-isolation sample-and-hold circuit which eliminates the glitches that occur whenever a DAC is dithered through a major carry. Su momentary transients can be of concern in applications such as high-resolution CRT beam positioning, where glitch-free code transitions are often required for optimum display qua ity and legibility. Oscilloscope photographs in Figures 7a and 7b below show the output of a DAC1136 being dithered up and down through the major carry, between codes 1000000000000000 and 0111111111111111. In Figure 7b, the Deglitcher IV is turned on virtually elminating the glitches and allowing the 152μV LSB step to be clearly seen.

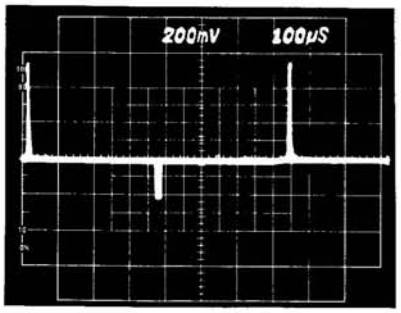


Figure 7a. DAC1136; Major-Carry Dither without Deglitch IV (BW = 1MHz), Vertical Scale 0.2V/Division

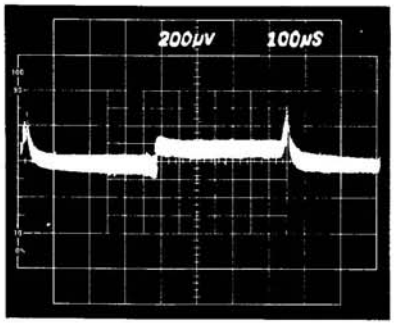


Figure 7b. Same Major-Carry Dither with Deglitcher IV (BW = 1MHz), Vertical Scale, 200μV/Division

The Deglitcher IV utilizes a proprietary sampling technique which isolates the output amplifier during the critical 10μs period immediately following a code change. The only discernible difference in DAC performance when used with Deglitcher IV is a delay of approximately 11μs after the strobe goes HI before the (deglitched) DAC output voltage starts slewing toward the new value.

GLITCH ADJUSTMENT

There are two "Glitch" adjustment potentiometers, accessible on the Card-Mounted Assembly. The adjustment on the card permits nulling of any Track-to-Hold offset, whereas th adjustment internal to the Deglitcher IV allows for precise nulling of the Hold-to-Track transient. Because of the near-infinite attenuation of the actual DAC current glitches, no current-glitch transient is visible on the output. For this reason, it is easiest to null the 2 Deglitcher adjustments whil strobing the Card with a static digital input.

INPUT OPTIONS

The Card-Mounted Assembly contains input registers. The input code ordered by the user is set at the factory by means of various jumpers in the logic circuitry. See ordering guide for details.

Since the Card-Mounted Assembly contains input registers, the card requires a strobe pulse circuit. Strobe characteristics of input registers are:

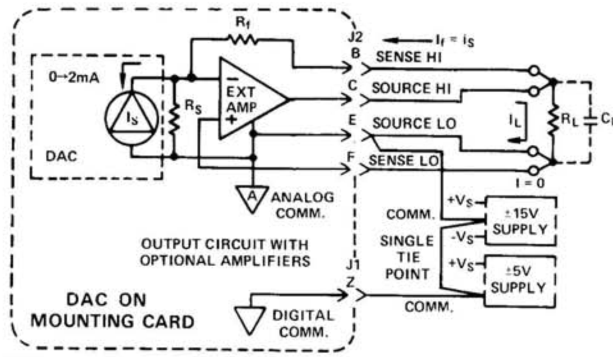
1. Strobe Pulse: One Std. series 74LS load, Leading-Edge-Triggered. Positive pulse should remain HI for > 100ns.
2. The digital input code can be changed at any time up to and including that instant when the strobe command goes HI.
3. The actual transfer of the input code to the DAC will occur ≈ 3μs after the strobe command; during this 3μs the digital input code to the card assembly should not be changed, in order to prevent the possible coupling of logic noise into the DAC output. At t_0 +3μs, the deglitcher is automatically enabled for the following ≈ 8μs. Thus there will be a delay of ≈ 11μs before the deglitched output starts slewing to the new value. Actual data transfer to the DAC automatically occurs at t_0 +3.1μs.

OUTPUT OPTIONS

The Card-Mounted Assembly for the DAC1136/1138 allows for several user-selectable output configurations:

1. Internal Output Amplifier inside the DAC Module.
2. Analog Devices model 234L; for low noise, low drift applications (2μV, ±0.1μV/°C).
3. Analog Devices model 44K; available only with DAC1136 recommended only for high speed or high current applications.
4. Deglitcher IV with self-contained precision BI-FET output amplifier (AD542K).
5. Deglitcher IV with model 234L output amplifier.
6. Deglitcher IV with model 44K output amplifier (recommer with DAC1136 only).

When using an external amplifier, a four terminal output connection can be utilized on the Card-Mounted Assembly in order to allow for compensation of connector contact resistance.



NOTE:
1. VOLTAGE DROP BETWEEN SOURCE LO AND SENSE LO MUST OBSERVE CURRENT MODE COMPLIANCE LIMITS FOR RATED ACCURACY.
2. THIS CONNECTION SCHEME CANNOT BE USED WITH INTERNAL AMPLIFIER OF THE DAC OR WITH THE AMPLIFIER INTERNAL TO THE DEGLITCHER IV.

Figure 8. Four-Terminal Output Connections

ORDERING GUIDE

WHEN ORDERING THE DAC1136 OR DAC1138, ORDER EITHER:

1. Module only: DAC1136J, DAC1136K, DAC1136L; DAC1138J, DAC1138K

2. DAC1136/1138 as a Card-Mounted Assembly:

DAC113 ☐ ☐ ☐ ☐ ☐ ☐

CODE	CODE	DAC MODULE RESOLUTION	DAC MODULE LINEARITY
6	J	16 BITS	15 BITS
6	K	16 BITS	16 BITS
6	L	16 BITS	16 BITS
8	J	18 BITS	17 BITS
8	K	18 BITS	18 BITS

CODE	OUTPUT AMPLIFIER
1	INTERNAL
2	44K[1]
3	234L
4	DEGLITCHER IV
5	DEGLITCHER IV[1] AND 44K
6	DEGLITCHER IV AND 234L

NOTE 1: NOT AVAILABLE FOR DAC1136L, DAC1138J AND DAC1138K.

CODE	INPUT LOGIC CODE
1	BIN/OBIN
2	COMP BIN/COMP OBIN
3	2'S COMP
4	COMP 2'S COMP
5	SIGN PLUS MAG BIN
6	COMP SIGN MAG BIN

CODE	OUTPUT VOLTAGE RANGE
1	+10V
2	±5V
3	±10V

CODE	DAC VOLTAGE REFERENCE
1	INTERNAL
2	EXTERNAL

Intronics Power ®

Low Cost/High Accuracy 18-Bit D/A Converter

DAC1146

FEATURES
- Integral Nonlinearity: ±0.00076% FSR max
- Differential Nonlinearity: ±0.00076% FSR max
- Low Differential Nonlinearity T.C.: ±1ppm/°C max
- Wide Power Supply Operation: ±11.5V to ±16V
- Fast Settling: 6µs to ±0.00076% FSR
- Small Size 2" × 2" × 0.4"

APPLICATIONS
- Automatic Test Equipment
- Digital Audio
- Sonar
- Robotics
- Nuclear Instrumentation

GENERAL DESCRIPTION

The DAC1146 is a low cost, 18-bit resolution (1 part in 262,144), digital-to-analog converter that provides high accuracy, high stability and is contained in a 2" × 2" × 0.4" module.

Integral and differential nonlinearity are both guaranteed at ±0.00076% FSR maximum. Additional guaranteed performance features include: differential nonlinearity T.C. ±1ppm/°C maximum, offset T.C. ±30µV/°C maximum, gain T.C. ±12ppm/°C maximum, bipolar offset T.C. ±7ppm/°C maximum.

The DAC1146 makes use of CMOS integrated circuits, thin-film resistor technology and proprietary CMOS current-steering switches to obtain high resolution, high reliability and small size. The calculated MTBF for the DAC1146 is 275,445 hours, per Mil Handbook 217C.

The DAC1146 can operate with power supplies ranging from ±11.5V to ±16.0V. An internal precision reference is provided, an external reference can be used. The external reference voltage input range is −12V to +12V. The analog output ranges include: +5V, +10V, ±5V, ±10V, −2mA and ±1mA, and are selectable via pin programming (see Figure 1). Digital input coding for unipolar operation is true binary, bipolar input coding is offset binary or 2's complement.

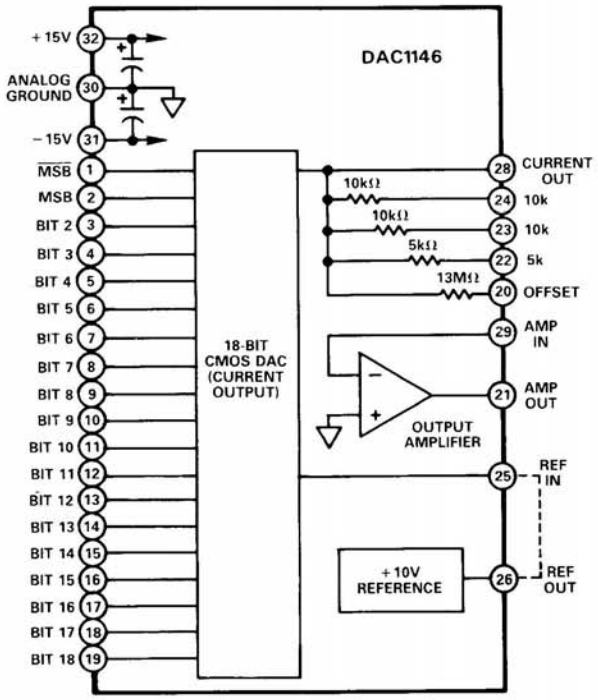


Figure 1. DAC1146 Functional Block Diagram

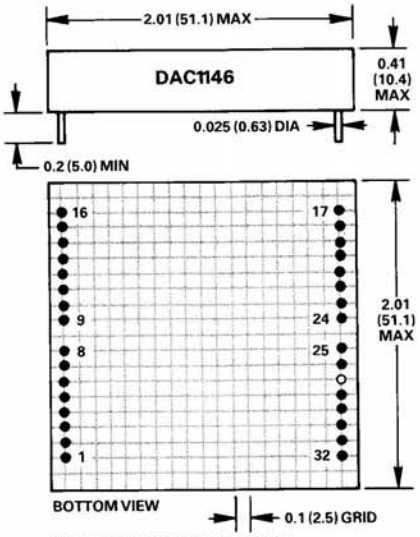
1400 PROVIDENCE HIGHWAY • BUILDING 2 NORWOOD, MASSACHUSETTS 02062-5015
PHONE: 781-551-5500 FAX: 781-551-5555

SPECIFICATIONS (typical @ +25°C, V_S = ±15V, V_{REF} = +10V unless otherwise specified)

MODEL	DAC1146
RESOLUTION	18 Bits
ACCURACY	
Integral Nonlinearity	± 0.00076% FSR[1](max)
Differential Nonlinearity	± 0.00076% FSR[1](max)
Monotonic (16 Bits)	Guaranteed
Offset[2]	Adjustable to Zero
Gain[2]	Adjustable to Full Scale
STABILITY	
Differential Nonlinearity	± 1ppm/°C (max)
Offset	± 30µV/°C (max)
Bipolar Offset	± 7ppm/°C (max)
Gain	± 12ppm/°C (max)
STABILITY, Long Term (ppm/1000 hr)	
Differential Nonlinearity	± 1ppm
Offset	± 3ppm
Bipolar Offset	± 3ppm
Gain	± 12ppm
REFERENCE VOLTAGE (V_{REF})	
Output Voltage	+ 10.00V ± 0.3% (max)
Output Current	2mA (max)
Ext. Ref Voltage Range[3]	− 12V to + 12V
Input Resistance	12kΩ
DYNAMIC PERFORMANCE[4]	
Settling Time to ± 0.00076% Voltage, Full Scale Step	
Unipolar (10V)	6µs
Bipolar (± 10V)	12µs
Voltage, LSB Step	3µs
Current	2µs
DIGITAL INPUTS	CMOS, TTL Compatible
Codes	
Unipolar	Binary (BIN)
Bipolar	Offset Binary (OBIN), Two's Complement
ANALOG OUTPUT	
Voltage	+ 5V, + 10V, ± 5V, ± 10V
Current	− 2mA, ± 1mA
Voltage Compliance	± 500mV
Noise (100kHz B.W.)	30µV rms
POWER REQUIREMENTS	
Voltage (Rated Performance)	± 15V (± 5%)
Voltage (Operating)	± 11.5V to ± 16.0V
Supply Current Drain ± 15V	+ 15mA, − 25mA
Total Power @ V_S = ± 15V	600mW
POWER SUPPLY SENSITIVITY	
Offset	0.001%/% ± V_S
Gain	0.001%/% ± V_S
TEMPERATURE RANGE	
Rated Performance	0 to + 70°C
Operating	− 25°C to + 85°C
Relative Humidity	Meets MIL STD 202E, Method 103B
SIZE	2" × 2" × 0.4" (50.8 × 50.8 × 10.16mm)
Weight	33g

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS

MATING CONNECTORS AC1584-3 (2 REQUIRED)

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{\text{MSB}}$	32	+15V
2	MSB	31	−15V
3	BIT 2	30	ANALOG GROUND
4	BIT 3	29	AMP IN
5	BIT 4	28	CURRENT OUT
6	BIT 5	27	N.C.
7	BIT 6	26	REFERENCE OUT
8	BIT 7	25	REFERENCE IN
9	BIT 8	24	10k
10	BIT 9	23	10k
11	BIT 10	22	5k
12	BIT 11	21	AMP OUT
13	BIT 12	20	OFFSET
14	BIT 13	19	BIT 18 (LSB)
15	BIT 14	18	BIT 17
16	BIT 15	17	BIT 16

NOTES
[1]FSR means Full Scale Range.
[2]Offset and gain are adjustable to zero by means of external potentiometers. See Figure 2 for proper connections.
[3]Rated performance is specified with + 10.0V reference.
[4]See Figure 5 for settling time curves.
Recommended Power Supply: Analog Devices Model 904.
Specifications subject to change without notice.

ANALOG OUTPUT RANGE

In the unipolar mode the DAC1146 provides an output current of −2mA. In the bipolar mode the DAC output current is offset by 1mA, (by connecting pin 25 to pin 24) for an output of ±1mA.

The DAC can be pin programmed for +5V, +10V, ±5V and ±10V by converting the DAC's current output to a voltage. To program the DAC for voltage output ranges (see Figure 1, Figure 2 and Table I).

Output Voltage Range	Input Code[1]	Connect Pin[2] 25 to Pin	Connect Pin 28 to Pin	Connect Pin 21 to Pin(s)
+5V	BIN		29	22, 23, 24
+10V	BIN		29	23, 24
±5V	OBIN, 2's Comp	24	29	22
±10V	OBIN, 2's Comp	24	29	23

[1]For BIN or OBIN codes connect $\overline{MSB}$ to ground.
For 2's comp code connect MSB to +5V system power.
[2]Connect Pin 25 through a 50Ω potentiometer to either internal reference (Pin 26) or an external reference.

Table I. Analog Output Range Pin Programming

OFFSET AND GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero by potentiometers as shown in Figure 2. Proper offset and gain calibration requires great care and the use of extremely sensitive and accurate measurement instruments. These instruments should be capable of measuring to within 1μV of the adjusted output voltage at both ends of the range. The potentiometers selected should be good quality Cermet type. Multi-turn potentiometers having ten to fifteen turns and 100ppm/°C temperature coefficients will be adequate. The temperature coefficients contributed by these Cermet potentiometers will be less than 0.1ppm/°C.

For unipolar mode, apply a digital input code of all "0's" and adjust the offset potentiometer until a 0.00000V output is obtained (see Table II). Once the appropriate offset adjustment has been made, apply a digital input code of all "1's", and adjust the gain potentiometer until the plus full scale output is obtained (see Table II).

For bipolar mode, apply a digital input code of 100 . . . 00 and adjust the offset potentiometer until a 0.00000V output is obtained (see Table II). Once the appropriate offset adjustment has been made, apply a digital input of all "1's", and adjust the gain potentiometer until the proper plus full scale output is obtained.

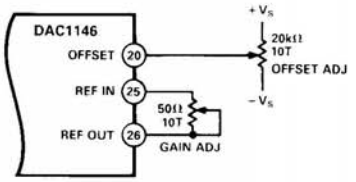


Figure 2. Offset & Gain Calibration

	Code 000 . . . 00	Code 111 . . . 11
Unipolar		
+5V	0.00000V	+4.999981V
+10V	0.00000V	+9.999962V
	Code 100 . . . 00	**Code 111 . . . 11**
Bipolar		
±5V	0.00000V	+4.999962V
±10V	0.00000V	+9.999924V

Table II. Full Scale Calibrated Output Voltages

PRECISION LOW DRIFT VOLTAGE OUTPUT

The internal output amplifier of the DAC1146 is optimized for high speed applications like digital audio and sonar, that require fast settling time. An external precision operational amplifier like the AD OP-07 can be applied when low offset drift is important. Simply connect the current output (Pin 28) to the inverting input of the amplifier. This connection should be made as close as possible to the DAC. Connect the proper feedback resistors as shown in last two columns of Table I. To avoid decreasing the gain drift performance of the DAC always use the internal feedback resistors, since they are matched to the internal current weighting resistors of the DAC (see Figure 3).

The current drift of the DAC1146 is typically 350pA/°C from +15°C to +35°C. When using the AD OP-07, the total drift of the output signal will be less than 2μV/°C.

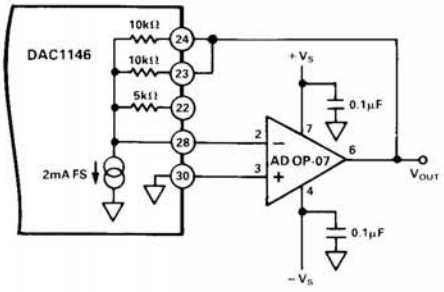


Figure 3. Low Drift Voltage Output (+10V) Application

DIFFERENTIAL LINEARITY ADJUSTMENT

Each DAC1146 has been factory calibrated and tested to achieve the performance indicated in the electrical specifications. Before attempting recalibration, it is imperative that the circuit be checked to confirm that all precautions have been taken to insure proper application. The DAC is trimmed by comparing a bit to the sum of all lower bits, and adjusted if necessary, for a one LSB positive difference. The top four bits can be trimmed using the procedure outlined on next page. A differential voltmeter capable of 100μV full scale should be connected to amp out of the DAC. A Fluke 895A or equivalent is recommended (see Figure 4).

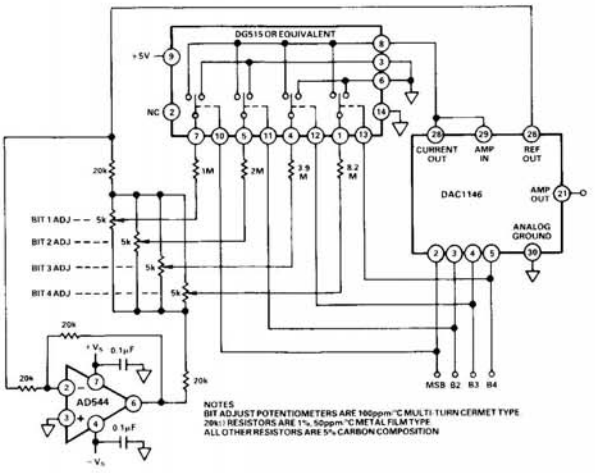


Figure 4. Optional Differential Linearity Adjustment Circuit

1. Start with Bit 4, proceed to Bits 3, 2 and 1 by repeating steps 2 through 5. Set Bits 17 and 18 to "0" for this entire rocedure.
2. Set all digital inputs less significant than the bit being adjusted to "1"; set all others to "0".
3. Read the output voltage by nulling the voltmeter.
4. Set the digital input for the bit being adjusted to "1", set all others to "0".
5. Read the output voltage by nulling the voltmeter. This reading should be equal to that of Step 3 plus 153μV (10V FSR). If not, adjust the bit.
6. Retrim gain.

DIGITAL AUDIO APPLICATION

When using a DAC to reconstruct an audio signal, emphasis is placed on important audio parameters. These parameters include: Total Harmonic Distortion, Dynamic Range and Settling Time.

Settling Time: Settling time is the total time for the output to settle within an error band around its final value after a change in the input. Settling times for the DAC1146 are specified to ±0.00076% of full-scale for any step change (see Figure 5).

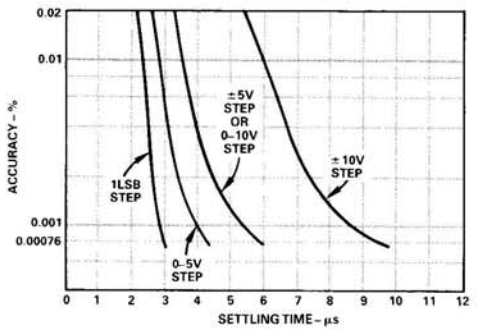


Figure 5. Voltage Settling Time vs Accuracy

Dynamic Range: The DAC1146 has a typical dynamic range of 96dB for a 16-bit input and 100dB for an 18-bit input. The theoretical dynamic range can be expressed as 6dB X N, where N is the number of bits. The theoretical limit would indicate a dynamic range of 108dB for an 18-bit input, however linearity, noise and other errors limit the useful dynamic range to 100dB at 18 bits.

Total Harmonic Distortion: When the DAC1146 is used at 16 bits of resolution with a deglitcher as shown in Figure 6, the Total Harmonic Distortion (THD) for a full scale signal over the entire audio range 20Hz to 20kHz is typically less than 0.002% or −94dB.

Total Harmonic Distortion is defined as the ratio of the square root of the sum of the squares of the rms harmonic value to the rms fundamental values and is expressed in percent dB.

The THD can be calculated from the following formula and verified by testing (see Figure 6).

$$THD = \frac{\text{RMS Error}}{\text{RMS Signal}} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}\left[E_L(i) + E_Q(i)\right]^2}}{\text{RMS Signal}} \times 100\%$$

where N is the number of samples.
$E_L(i)$ is the linearity error of the DAC at each sample point.
$E_Q(i)$ is the quantization error of the DAC at each sample point.

THD TESTING

When testing for THD the test equipment used must be distortion free so as not to mask the true performance of the device under test. The test circuit (see Figure 6) will produce a negligible amount of distortion when generating a test signal.

The PROM contains one cycle of a computer generated sine wave. Frequency select switches program the adder with the number of codes that it should skip on each count. This selection allows any of 2048 discrete frequencies between 12Hz and 25kHz to be generated with a constant 50kHz update rate. The DAC output is deglitched, and displayed on the spectrum analyzer. Total Harmonic Distortion can be computed by comparing the amplitude of the fundamental frequency with the amplitudes of the harmonics.

TYPICAL THD TEST RESULTS

Dynamic Range	16-Bit Resolution	18-Bit Resolution
Dynamic Range	96dB	100dB
THD at FS	0.002% (−94dB)	0.0015% (−96dB)
THD at −15dB	0.01% (−80dB)	0.0075% (−82dB)
THD at −20dB	0.02% (−74dB)	0.015% (−76dB)
THD at −30dB	0.06% (−64dB)	0.045% (−67dB)

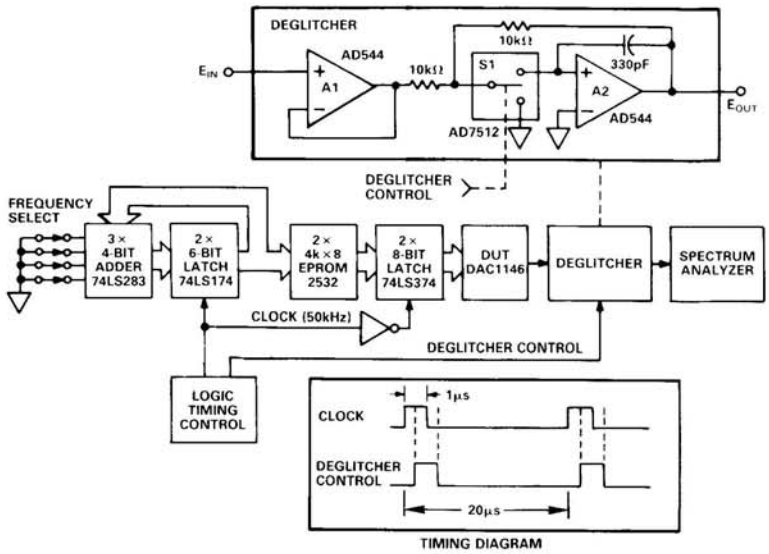


Figure 6. Block Diagram Harmonic Distortion Test Circuit

Intronics Power ®

14-Bit & 15-Bit Sampling Analog To Digital Converter

DAS1152/DAS1153

FEATURES

- Complete with High Accuracy Sample/Hold and A/D Converter
- Differential Nonlinearity: ±0.002% FSR max (DAS1153)
- Nonlinearity: DAS1152: ±0.005% FSR max
  DAS1153: ±0.003% FSR max
- Low Differential Nonlinearity T.C.: ±2ppm/°C max
- High Throughput Rate: 25kHz min (DAS1152)
- High Feedthrough Rejection: −96dB
- Byte-Selectable Tri-State Buffered Outputs
- Internal Gain & Offset Potentiometers
- Improved Second Source to A/D/A/M 824 and A/D/A/M 825 Modules
- Low Cost

APPLICATIONS

- Process Control Data Acquisition
- Automated Test Equipment
- Seismic Data Acquisition
- Nuclear Instrumentation
- Medical Instrumentation
- Robotics

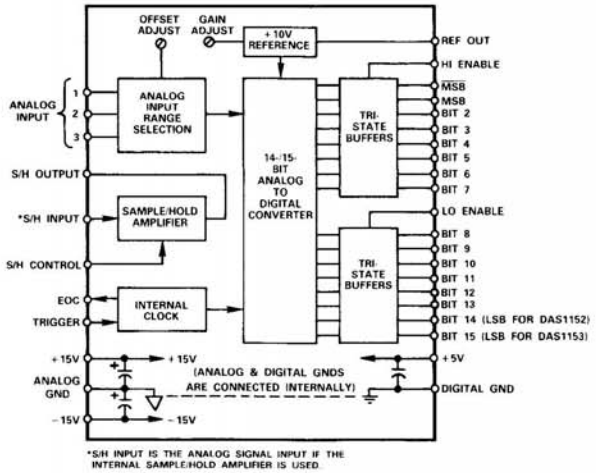


Figure 1. DAS1152/DAS1153 Block Diagram

GENERAL DESCRIPTION

The DAS1152/DAS1153 are 14-/15-bit sampling analog-to-digital converters having a maximum throughput rate of 25kHz/20kHz. They provide high accuracy, high stability, and functional completeness all in a 2″ × 4″ × 0.44″ metal case.

Guaranteed high accuracy system performance such as nonlinearity of ±0.005% FSR (DAS1152)/±0.003% FSR (DAS1153) and differential nonlinearity of ±0.003% FSR (DAS1152)/±0.002% FSR (DAS1153) are provided. Guaranteed stability such as differential nonlinearity T.C. of ±2ppm/°C (DAS1153) maximum, zero T.C. of ±80μV/°C maximum, gain T. C. of ±8ppm/°C maximum and power supply sensitivity of ±0.001% FSR/% V_S are also provided by the DAS1152/DAS1153.

The DAS1152/DAS1153 make extensive use of both integrated circuit and thin film components to obtain their excellent performance, small size, and low cost. The devices contain a precision sample/hold amplifier, high accuracy 14-/15-bit analog-to-digital converter, tri-state output buffers, internal gain and offset trim potentiometers, and power supply bypass capacitors (as shown in Figure 1).

Four analog input voltage ranges are selectable via user pin programming: 0 to +5V, 0 to +10V, ±5V, and ±10V. Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement. Tri-state buffers provide easy interface to bus structured applications.

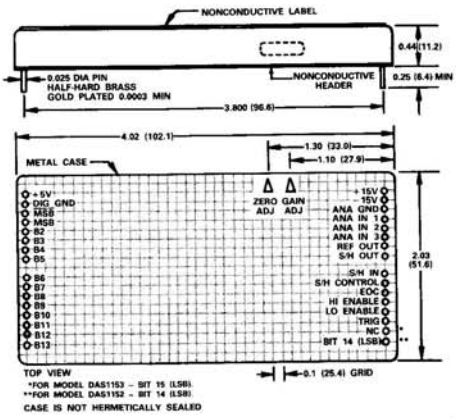
1400 PROVIDENCE HIGHWAY • BUILDING 2 NORWOOD, MASSACHUSETTS 02062-5015
PHONE: 781-551-5500 FAX: 781-551-5555

SPECIFICATIONS (typical @ +25°C unless otherwise specified)

MODEL	DAS1152	DAS1153
RESOLUTION	14 Bits	15 Bits
DYNAMIC PERFORMANCE		
Throughput Rate	25kHz min	20kHz min
Conversion Time	35µs max	44µs max
S/H Acquisition Time	4µs max	5µs max
S/H Aperture Delay	50ns	*
S/H Aperture Uncertainty	1ns	*
Feedthrough Rejection[1]	−96dB	*
Droop Rate	0.05µV/µs (0.1µV/µs max)	*
Dielectric Absorption Error	±0.005% of Input Voltage Change	*
ACCURACY		
Integral Nonlinearity[2]	±0.005% FSR[3] max	±0.003% FSR[3] max
Differential Nonlinearity	±0.003% FSR[3] max	±0.002% FSR[3] max
No Missing Codes	Guaranteed	*
±3σ Noise (S/H plus A/D)	75µV rms	*
±3σ Noise (A/D)	50µV rms	*
STABILITY		
Differential Nonlinearity T.C.	±2ppm/°C max	*
Gain T.C.	±8ppm/°C max	*
Zero T.C.	±30µV/°C typ, ±80µV/°C max	*
Power Supply Sensitivity	±0.001% FSR[3]/% V_s	*
ANALOG INPUT		
Voltage Range		
Bipolar	±5V, ±10V	*
Unipolar	0 to +5V, 0 to +10V	*
ADC Input Impedance 0 to +5V	2.5kΩ	*
0 to +10V, ±5V	5kΩ	*
±10V	10.0kΩ	*
S/H Input Impedance	100MΩ‖5pF	*
DIGITAL INPUTS		
Convert Command[4]	1TTL Load, Positive Pulse	*
	Negative Edge Triggered	*
S/H Control	HOLD = Logic 0	*
	SAMPLE = Logic 1	*
Low Enable, High Enable	ENABLE = Logic 0	*
DIGITAL OUTPUTS		
Parallel Data Outputs		
Unipolar	Binary	*
Bipolar	Offset Binary, 2's Complement	*
Output Drive	2TTL Loads	*
Status	Logic "1" During Conversion	*
Output Drive	2TTL Loads	*
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%	*
External Load Current (Rated Performance)	2mA max	*
Temperature Stability	±5ppm/°C max	*
POWER REQUIREMENTS		
Rated Voltages	±15V (±3%), +5V (±5%)	*
Operating Voltages[5]	±12V to +17V, +4.75V to +5.25V	*
Supply Current Drain ±15V	±37mA	*
+5V	80mA	*
TEMPERATURE RANGE		
Specified	0 to +70°C	*
Operating	−25°C to +85°C	*
Storage	−25°C to +85°C	*
Relative Humidity	Meets MIL-STD-202E, Method 103B	*
Shielding	Electrostatic (RFI) 6 Sides,	*
	Electromagnetic (EMI) 5 Sides	*
SIZE	2" × 4" × 0.44" Metal Package	*

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES

*Specifications same as DAS1152

[1]Measured in hold mode, input 20V pk-pk @ 10kHz.

[2]Worst-case summation of S/H and A/D nonlinearity errors.

[3]FSR means Full Scale Range.

[4]When connecting the Convert Command and the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy 4µs (max, DAS1152)/5µs (max, DAS1153). If the A/D converter is only used, the Convert Command pulse width should be 100ns min (see Figure 2).

[5]If only the ADC portion is used, the operating power supply voltage can be maintained at ±12V to ±17V. But if the S/H section is required, the operating voltage must be maintained at ±15V (±3%) or the S/H input voltage must be limited to −7V to +10V for a ±12V supply voltage.

[6]Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

OPERATION

The DAS1152/DAS1153 are functionally complete data acquisition subsystems being fully characterized as such. All the necessary data acquisition and microprocessor interface elements are provided internal to these devices. Accuracy and performance criteria are tested and specified for the entire system. Thus, design time and associated high accuracy problems are minimized because layout and component optimization have already been performed.

For operation, the only connections necessary to the DAS1152/DAS1153 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Analog input and digital output programming are user selectable via external jumper connections.

ANALOG INPUT SECTION

The analog input can be applied to just the A/D converter or to the internal sample/hold amplifier ahead of the A/D converter. When using just the A/D converter, apply the analog input per the voltage range pin programming shown in Table 1. When using the sample/hold amplifier in conjunction with A/D converter, apply the analog input to the S/H INPUT terminal and connect the S/H OUTPUT terminal to the appropriate A/D converter analog input.

Analog Voltage Input Range	Connect V_{IN} or S/H Out To	Connect Analog Common To	Connect Ref Out To
0 to +5V	ANA IN 1, ANA IN 2, ANA IN 3	Ground	NC*
0 to +10V	ANA IN 2 ANA IN 3	Ground ANA IN 1	NC*
±5V	ANA IN 1	Ground, ANA IN 3	ANA IN 2
±10V	ANA IN 3	Ground, ANA IN 1	ANA IN 2

*No Connection

Table 1. Analog Input Pin Programming

Errors due to source loading are eliminated since the sample/hold amplifier is a high-impedance unity-gain amplifier. High feedthrough rejection is provided for either single-channel or multichannel applications. Feedthrough rejection can be optimized, in multichannel applications, by changing channels at the rising or falling edge of the S/H control pulse.

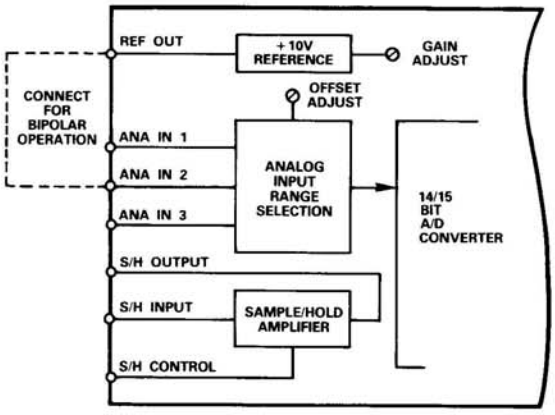


Figure 2. Analog Input Block Diagram

TIMING DIAGRAM

The timing diagram for the DAS1152/DAS1153 is illustrated in Figure 3. This figure also includes the sample/hold amplifier acquisition time.

If the sample/hold amplifier is required, the TRIGGER input and S/H CONTROL terminal can be tied together providing only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of 4μs (DAS1152)/5μs (DAS1153) to insure accuracy is attained. If the sample/hold amplifier is not used, the trigger pulse needs to be only 100ns (min) in length to satisfy the A/D converter trigger requirements. At the falling edge of the trigger pulse, the sample/hold amplifier is placed in the hold mode, the A/D conversion begins, and all internal logic is reset. Once the conversion process is initiated, it cannot be retriggered until after the end of conversion.

With this negative edge of the trigger pulse the MSB is set low with the remaining digital outputs set to logic high state, and the status line is set high and remains high through the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched low at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-bit conversion taking 35μs/44μs maximum for the DAS1152/DAS1153 respectively. At this time, the STATUS line goes low signifying that the conversion is complete. For microprocessor bus applications, the digital output can now be applied to the data bus by enabling the tri-state buffers. For maximum data throughput, the digital output data should be read while the sample/hold amplifier is acquiring the new analog input signal.

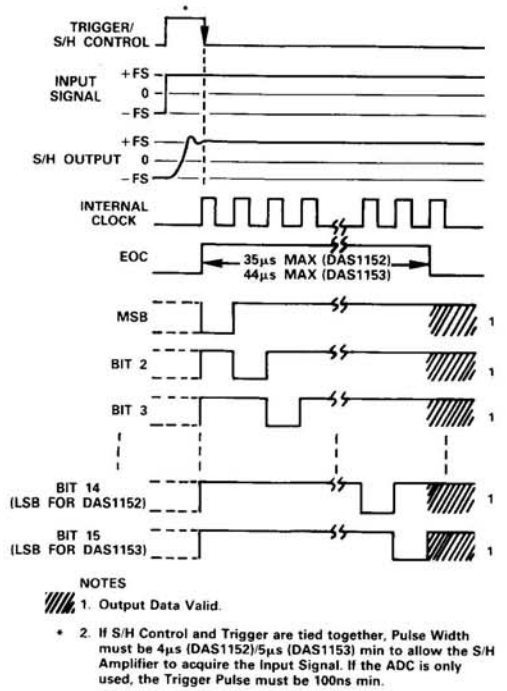


Figure 3. DAS1152/DAS1153 Timing Diagram

GAIN AND OFFSET ADJUSTMENT

The DAS1152/DAS1153 contain internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Since offset calibration is not affected by changes in gain calibration, it should be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within ±1/10LSB of the desired value at any point within its range.

OFFSET CALIBRATION

For a 0 to +10V unipolar range set the input voltage precisely to +305μV for the DAS1152 and +153μV for the DAS1153. For a 0 to +5V unipolar range set the input to +153μV for the DAS1152 and +76μV for the DAS1153. Then adjust the zero potentiometer until the converter is just on the verge of switching from 000.....000 to 000.....001.

For the ±5V bipolar range set the input voltage precisely to +305μV for the DAS1152 and +153μV for the DAS1153. For a ±10V bipolar range set the input voltage precisely to +610μV for the DAS1152 and +305μV for the DAS1153. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000.....000 to 000.....001 and the two's complement coded units are just on the verge of switching from 100.....000 to 100.....001.

GAIN CALIBRATION

Set the input voltage precisely to +9.99909V (DAS1152)/ +9.99954V (DAS1153) for the 0 to +10V units, +4.99954V (DAS1152)/+4.99977V (DAS1153) for 0 to +5V units, +9.99817V (DAS1152)/+9.99909V (DAS1153) for ±10V units, or +4.99909V (DAS1152)/+4.99954V (DAS1153) for ±5V units. Note that these values are 1 1/2LSBs less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11.....10 to 11.....11 and two's complement coded units are just on the verge of switching from 011.....10 to 011.....11.

DAS1152/DAS1153 INPUT/OUTPUT RELATIONSHIPS

The DAS1152/DAS1153 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary codes while ($\overline{\text{MSB}}$) is used to obtain two's complement coding. Table 2 shows the DAS1152/DAS1153 unipolar analog input/digital output relationships. Tables 3 and 4 show the DAS1152/DAS1153 bipolar analog input/digital output relationships.

NOMINAL BIPOLAR INPUT-OUTPUT RELATIONSHIPS

ANALOG INPUT			
0 to +5V Range		0 to +10V Range	
DAS1152	DAS1153	DAS1152	DAS1153
+4.99969V	+4.99984V	+9.99939V	+9.99969V
+2.50000V	+2.50000V	+5.0000V	+5.00000V
+0.62500V	+0.62500V	+1.25000V	+1.25000V
+0.0003V	+0.00015V	+0.0006V	+0.0003V
+0.0000V	+0.0000V	+0.0000V	+0.0000V

DIGITAL OUTPUT	
Binary Code	
DAS1152	DAS1153
11 111 111 111 111	111 111 111 111 111
10 000 000 000 000	100 000 000 000 000
00 100 000 000 000	001 000 000 000 000
00 000 000 000 001	000 000 000 000 001
00 000 000 000 000	000 000 000 000 000

Table 2. Unipolar Input-Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.99939V	+9.99878V	11 111 111 111 111	01 111 111 111 111
+2.50000V	+5.0000V	11 000 000 000 000	01 000 000 000 000
+0.00061V	+0.00122V	10 000 000 000 001	00 000 000 000 001
+0.00000V	+0.00000V	10 000 000 000 000	00 000 000 000 000
−5.00000V	−10.00000V	00 000 000 000 000	10 000 000 000 000

Table 3. DAS1152 Bipolar Input/Output Relationships

Analog Input		Digital Output	
±5V Range	±10V Range	Offset Binary Code	Two's Complement Code
+4.99969V	+9.99939V	111 111 111 111 111	011 111 111 111 111
+2.50000V	+5.0000V	110 000 000 000 000	010 000 000 000 000
+0.0003V	+0.00061V	100 000 000 000 001	000 000 000 000 001
+0.00000V	+0.00000V	100 000 000 000 000	000 000 000 000 000
−5.00000V	−10.00000V	000 000 000 000 000	100 000 000 000 000

Table 4. DAS1153 Bipolar Input/Output Relationships

TRI-STATE DIGITAL OUTPUT

The ADC digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data bus in either a one-byte or a two-byte format by using the HIGH BYTE ENABLE and LOW BYTE ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

POWER SUPPLY AND GROUNDING CONNECTIONS

Although the analog power ground and the digital ground are connected in the DAS1152/DAS1153, care must still be taken to provide proper grounding due to the high accuracy nature of these devices. Though only general guidelines can be given, grounding should be arranged in such a manner as to avoid ground loops and to minimize the coupling of voltage drops (on the high current carrying logic supply ground) to the sensitive analog circuit sections. Analog and digital grounds should remain separated on the PC board and terminated at the respective DAS1152/DAS1153 terminals.

No power supply decoupling is required since, the DAS1152/ DAS1153, contain high quality tantalum capacitors on each of the power supply inputs to ground.

Intronics Power ®

Low Power 14-Bit, 15-Bit & 16-Bit Sampling Analog-to-Digital Converters

DAS1157/DAS1158/DAS1159

FEATURES

- Complete with High Accuracy Sample/Hold and A/D Converter
- Low Power Consumption: 650mW max, $V_S = \pm 15V$
- Rated Performance: −25°C to +85°C
- Low Nonlinearity (DAS1158 and DAS1159)
  - Differential: ±0.0015% FSR max
  - Integral: ±0.003% FSR max
  - Differential T.C.: ±1ppm/°C max
- High Throughput Rate: 18kHz min
- Byte-Selectable Tri-State Buffered Outputs
- Internal Gain & Offset Potentiometers
- All Hermetically-Sealed Semiconductors
- Improved Second Source to A/D/A/M-834 and A/D/A/M-835 Modules

APPLICATIONS

- Seismic Data Acquisition
- Portable Field Instrumentation
- Automated Test Equipment
- Process Control Data Acquisition
- Medical Instrumentation

GENERAL DESCRIPTION

The DAS1157/DAS1158/DAS1159 are 14-/15-/16-bit sampling analog-to-digital converters. They are ideally suited for use in portable and remote data acquisition equipment where low power consumption (650mW maximum) and wide temperature range (−25°C to +85°C rated performance) are required.

DAS1157/DAS1158/DAS1159 provide guaranteed high accuracy and high stability system performance essential to medical, analytical and process control equipment: differential nonlinearity of ±0.0015% max and integral nonlinearity of ±0.003% max (DAS1158 and DAS1159); no missing codes guaranteed; gain T.C. of ±8ppm/°C max, zero T.C. of ±80μV/°C max and differential nonlinearity T.C. of ±1ppm/°C max.

The wide dynamic range will enhance the performance of critical measurements in gas and liquid chromatography, blood analyzers, distributed data acquisition in factory automation and power generating equipment, and in automatic test equipment.

The DAS1157/DAS1158/DAS1159 make use of Analog Devices' proprietary CMOS technology to achieve low power operation, while utilizing the latest integrated circuit and thin-film components to achieve the highest level of performance and reliability. All hermetically-sealed semiconductor components are used to insure added reliability over a wide range of operating conditions.

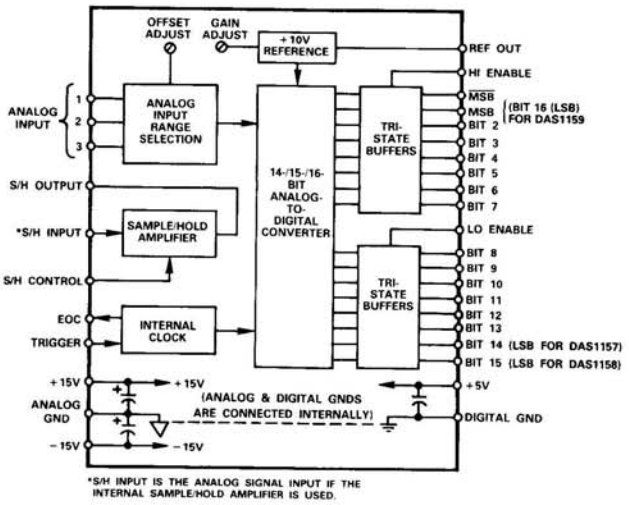


Figure 1. DAS1157/DAS1158/DAS1159 Block Diagram

As shown in Figure 1, each device contains a precision sample/hold amplifier, high accuracy 14-/15-/16-bit analog-to-digital converter, precision reference, CMOS tri-state output buffers (for direct 8-bit or 16-bit bus interface), user accessible gain and offset adjust potentiometers, and power supply bypass capacitors, all in a compact low profile 2″ × 4″ × 0.375″ metal case package. No additional components are required for operation.

1400 PROVIDENCE HIGHWAY • BUILDING 2 NORWOOD, MASSACHUSETTS 02062-5015
PHONE: 781-551-5500 FAX: 781-551-5555

SPECIFICATIONS (typical @ +25°C, V_S = ±15V, V_D = +5V unless otherwise specified)

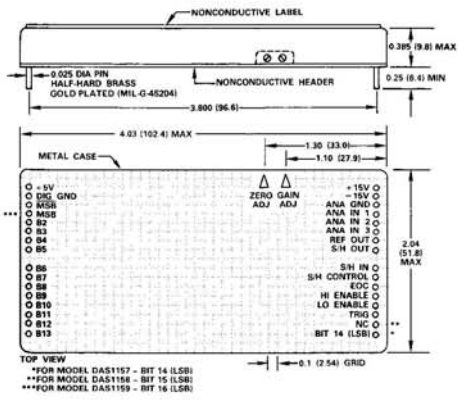
MODEL	DAS1157	DAS1158	DAS1159
RESOLUTION	14 Bits	15 Bits	16 Bits
DYNAMIC PERFORMANCE			
Throughput Rate	18kHz min	*	*
Conversion Time	50µs max	*	*
S/H Acquisition Time	5µs max	*	*
S/H Aperture Delay	250ns	*	*
S/H Aperture Uncertainty	1ns	*	*
Feedthrough Rejection[1]	−90dB min	*	*
Droop Rate	0.05µV/µs, 0.1µV/µs max	*	*
Dielectric Absorption Error	±0.005% of Input Voltage Change	*	*
ACCURACY			
Integral Nonlinearity[2]	±0.005% FSR[3] max	±0.003% FSR[3] max	**
Differential Nonlinearity[4]	±0.003% FSR[3] max	±0.0015% FSR[3] max	**
No Missing Codes	Guaranteed	*	*
±3σ Noise (S/H plus A/D)	0.0022% p-p (75µV rms)	*	*
±3σ Noise (A/D)	0.0015% p-p (50µV rms)	*	*
STABILITY			
Differential Nonlinearity T.C.	±2ppm/°C max	±1ppm/°C max	**
Gain T.C.	±8ppm/°C max	*	*
Zero T.C.	±30µV/°C typ, ±80µV/°C max	*	*
Conversion Time T.C.	±0.05%/°C	*	*
Power Supply Sensitivity	±0.001% FSR[3]/% V_S	*	*
Warm-Up Time	Less than 1 Minute	*	*
ANALOG INPUT			
Voltage Range			
Bipolar	±5V, ±10V	*	*
Unipolar[4]	0 to +5V, 0 to +10V	*	*
ADC Input Impedance 0 to +5V	2.5kΩ	*	*
0 to +10V, ±5V	5kΩ	*	*
±10V	10kΩ	*	*
S/H Input Impedance	100MΩ‖5pF	*	*
DIGITAL INPUTS			
A/D Trigger[5]	Positive Pulse, Neg. Edge Triggered	*	*
Logic Levels	5V CMOS Compatible	*	*
S/H Control	SAMPLE = Logic 1, TTL Compatible	*	*
Low Enable, High Enable[6]	ENABLE = Logic 0, CMOS/TTL Compatible	*	*
DIGITAL OUTPUTS			
Parallel Data Outputs			
Unipolar	Binary	*	See Note 7
Bipolar	Offset Binary, 2's Complement	*	See Note 7
Output Drive	2TTL Loads	*	*
End of Conversion	Logic "1" During Conversion	*	*
Output Drive	2TTL Loads	*	*
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%	*	*
External Load Current (Rated Performance)	2mA max	*	*
POWER REQUIREMENTS			
Rated Voltages	±15V (±3%), +5V (±5%)	*	*
Operating Voltages[8,9]	±12V to ±17V, +4.75V to +5.25V	*	*
Supply Current Drain ±15V	±15mA	*	*
+5V	10mA	*	*
Total Power Consumption, V_S = ±15V	500mW typ, 650mW max	*	*
TEMPERATURE RANGE			
Rated Performance	−25°C to +85°C	*	*
Operating	−25°C to +85°C	*	*
Storage	−40°C to +100°C	*	*
Relative Humidity	Meets MIL-STD-202E, Method 103B	*	*
Shielding	Electrostatic (RFI) 6 Sides	*	*
	Electromagnetic (EMI) 5 Sides	*	*
SIZE	2" × 4" × 0.375" Metal Package	*	*

NOTES
*Specifications same as DAS1157
**Specifications same as DAS1158
[1]Measured in hold mode, input 20V pk-pk @ 10kHz.
[2]Worst-case summation of S/H and A/D nonlinearity errors.
[3]FSR means Full Scale Range.
[4]Differential Nonlinearity in the 0 to +5V input range is specified as ±0.003% typical for the DAS1157, DAS1158 and DAS1159.
[5]When connecting the Trigger and the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy (5µs min). If the A/D converter only is used, the Trigger pulse width should be 1µs min (see Figure 3).
[6]Low Byte Enable pin connections are Bits 8 through 15; High Byte Enable pin connections are MSB, MSB or Bit 16 and Bits 2 through 7.
[7]DAS1159 unipolar coding is provided in a modified binary format (MSB complement) while bipolar coding is two's complement only. The MSB must be inverted for binary and offset binary codes.
[8]When the S/H section is required, $-V_S$ must be at least 5 volts more negative than the most negative analog input voltage (example: V_S = +12V dc, therefore, maximum analog input is +10 and −7V).
[9]Recommended Power Supply: Analog Devices Model 923.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ASSEMBLY INSTRUCTIONS

CAUTION: This module is not an embedded assembly and is not hermetically sealed. Do not subject to a solvent or water-wash process that would allow direct contact with free liquids or vapors. Entrapment of contaminants may occur, causing performance degradation and permanent damage. Install after any clean/wash process and then only spot clean by hand.

OPERATION

For operation, the only connections necessary to the DAS1157/DAS1158/DAS1159 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Analog input and digital output programming are user selectable via external jumper connections.

Input voltage ranges are selectable via user pin programming: 0 to +5V, 0 to +10V, ±5V and ±10V. Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement (DAS1157 and DAS1158). DAS1159 unipolar coding is provided in a modified binary format (MSB complement) while bipolar coding is two's complement only.

ANALOG INPUT SECTION

The analog input can be applied to just the A/D converter or to the internal sample/hold amplifier ahead of the A/D converter. When using just the A/D converter, apply the analog input per the voltage range pin programming shown in Table I. When using the sample/hold amplifier in conjunction with A/D converter, apply the analog input to the S/H INPUT terminal and connect the S/H OUTPUT terminal to the appropriate A/D converter analog input.

Analog Voltage Input Range	Connect V_{IN} or S/H Out To	Connect Analog Common To	Connect Ref Out To
0 to +5V	ANA IN 1, ANA IN 2, ANA IN 3	Ground	NC*
0 to +10V	ANA IN 2 ANA IN 3	Ground ANA IN 1	NC*
±5V	ANA IN 1	Ground, ANA IN 3	ANA IN 2
±10V	ANA IN 3	Ground, ANA IN 1	ANA IN 2

*No Connection

Table I. Analog Input Pin Programming

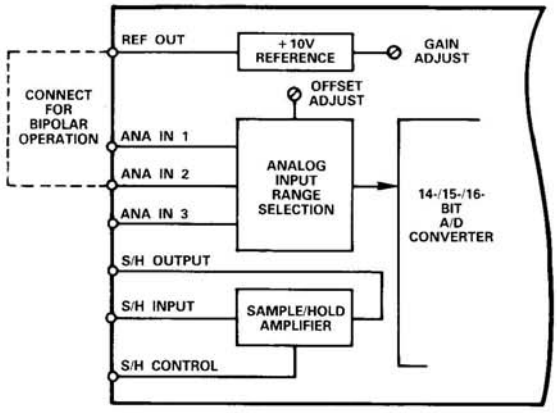


Figure 2. Analog Input Block Diagram

Errors due to source loading are eliminated since the sample/hold amplifier is a high-impedance unity-gain amplifier. High feedthrough rejection is provided for either single-channel or multichannel applications. Feedthrough rejection can be optimized, in multichannel applications, by changing channels at the rising or falling edge of the S/H control pulse.

TIMING DIAGRAM

The timing diagram for the DAS1157/DAS1158/DAS1159 is illustrated in Figure 3. This figure also includes the sample/hold amplifier acquisition time.

If the sample/hold amplifier is required, the TRIGGER input and S/H CONTROL terminal can be tied together providing only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of 5µs to insure accuracy. If the sample/hold amplifier is not used, the trigger pulse needs to be 1µs (minimum) in length to satisfy the A/D converter trigger requirements. At the falling edge of the trigger pulse, the sample/hold amplifier is placed in the hold mode, all internal logic is reset and the A/D conversion begins. The conversion process can be retriggered at any time, including during conversion.

With this negative edge of the trigger pulse, the MSB is set high with the remaining digital outputs set to logic low state, and the end of conversion is set high and remains high through the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched high at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-/16-bit conversion taking 50µs maximum. At this time, the end of conversion line goes low signifying that the conversion is complete. For microprocessor bus applications, the digital output can now be applied to the data bus by enabling the tri-state buffers. For maximum data throughput, the digital output data should be read while the sample/hold amplifier is acquiring the new analog input signal.

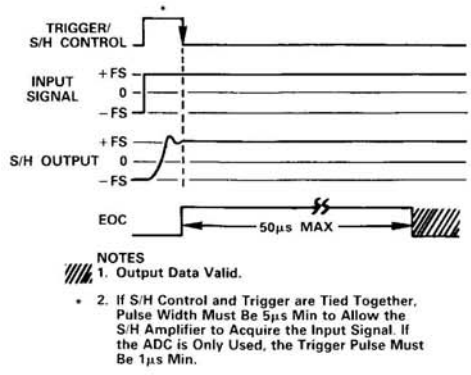


Figure 3. DAS1157/DAS1158/DAS1159 Timing Diagram

GAIN AND OFFSET ADJUSTMENT

The DAS1157/DAS1158/DAS1159 contain internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Offset calibration is not affected by changes in gain calibration, and should be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within ±1/10LSB of the desired value at any point within its range.

OFFSET CALIBRATION

For a 0 to +10V unipolar range, set the input voltage precisely to +305μV for the DAS1157, +153μV for the DAS1158 and +76μV for the DAS1159. For a 0 to +5V unipolar range, set the input to +153μV for the DAS1157, +76μV for the DAS1158 and +38μV for the DAS1159. Then adjust the zero potentiometer until the converter is just on the verge of switching from 000.....000 to 000.....001 (DAS1157/DAS1158) or from 100.....000 to 100.....001 (DAS1159).

For the ±5V bipolar range, set the input voltage precisely to +305μV for the DAS1157, +153μV for the DAS1158 and +76μV for the DAS1159. For a ±10V bipolar range, set the input voltage precisely to +610μV for the DAS1157, +305μV for the DAS1158 and +153μV for the DAS1159. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000.....000 to 000.....001 and the two's complement coded units are just on the verge of switching from 100.....000 to 100.....001.

GAIN CALIBRATION

Set the input voltage precisely to +9.99909V (DAS1157)/ +9.99954V (DAS1158)/+9.99977V (DAS1159) for the 0 to +10V units, +4.99954V (DAS1157)/+4.99977V (DAS1158)/ +4.99989V (DAS1159) for 0 to +5V units, +9.99817V (DAS1157)/+9.99909V (DAS1158)/+9.99954V (DAS1159) for ±10V units, or +4.99909V (DAS1157)/+4.99954V (DAS1158)/ +4.99977V (DAS1159) for ±5V units. Note that these values are 1 1/2LSBs less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11.....10 to 11.....11 or modified binary and two's complement coded units are just on the verge of switching from 011.....10 to 011.....11.

DAS1157/DAS1158/DAS1159 INPUT/OUTPUT RELATIONSHIPS

The DAS1157/DAS1158 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary codes while ($\overline{\text{MSB}}$) is used to obtain two's complement coding. The DAS1159 produces a modified binary coded output when configured as a unipolar device. Configured as a bipolar device it can only produce two's complement output codes. The DAS1159 uses $\overline{\text{MSB}}$ to obtain the modified binary and two's complement output codes; the DAS1159 does not have an MSB output. Table II shows the DAS1157/ DAS1158/DAS1159 unipolar analog input/digital output relationships. Table III shows the DAS1157/DAS1158/DAS1159 bipolar analog input/digital output relationships.

Input Voltage – Output Code Relationships

Unipolar Input Voltages

Analog Input		Digital Output
0 to +5V Range	**0 to +10V Range**	
DAS1157		Binary Code
+4.99969V	+9.99939V	11 1111 1111 1111
+0.00000V	+0.00000V	00 0000 0000 0000
DAS1158		Binary Code
+4.99985V	+9.99969V	111 1111 1111 1111
+0.00000V	+0.00000V	000 0000 0000 0000
DAS1159		Modified Binary Code
+4.99992V	+9.99985V	0111 1111 1111 1111
+0.00000V	+0.00000V	1000 0000 0000 0000

Table II. Unipolar Input-Output Relationships

Bipolar Input Voltages

Analog Input		Digital Output	
±5V Range	**±10V Range**	**Offset Binary Code**	**Two's Complement Code**
DAS1157			
+4.99939V	+9.99878V	11 1111 1111 1111	01 1111 1111 1111
+0.00000V	+0.00000V	10 0000 0000 0000	00 0000 0000 0000
−5.00000V	−10.00000V	00 0000 0000 0000	10 0000 0000 0000
DAS1158			
+4.99969V	+9.99939V	111 1111 1111 1111	011 1111 1111 1111
+0.00000V	+0.00000V	100 0000 0000 0000	000 0000 0000 0000
−5.00000V	−10.00000V	000 0000 0000 0000	100 0000 0000 0000
DAS1159			
+4.99985V	+9.99969V		0111 1111 1111 1111
+0.00000V	+0.00000V		0000 0000 0000 0000
−5.00000V	−10.00000V		1000 0000 0000 0000

Table III. Bipolar Input-Output Relationships

TRI-STATE DIGITAL OUTPUT

The ADC digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data bus in either a one-byte or a two-byte format by using the HIGH BYTE ENABLE and LOW BYTE ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

POWER SUPPLY AND GROUNDING CONNECTIONS

No power supply decoupling is required since the DAS1157/ DAS1158/DAS1159 contain high quality tantalum capacitors on each of the power supply inputs to ground.

The analog and digital grounds are internally connected in the DAS1157/DAS1158/DAS1159. But in many applications, an external connection between the digital ground pin and analog ground pin is advisable for optimum performance.

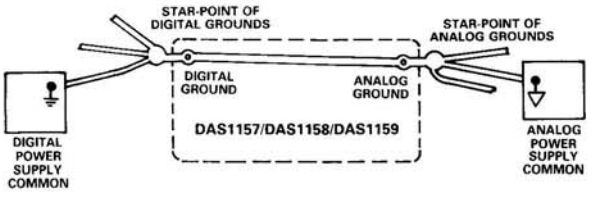


Figure 4. Typical Ground Layout for DAS1157/DAS1158/ DAS1159